Chapter 9
Nanotechnology for Computers, Memories, and Hard Disks

The field of computer and data storage development is of particular importance in nanoscience. The design and fabrication of computer components, such as transistors, or of data bits in storage media are governed by the principles of physics, chemistry, and materials science on the nanoscale. On the other hand, the nanotechnical semiconductor industry with its current revenues of ∼200 billion US $ annually [9.1] is presumably the largest economic factor where nanotechnology plays a central role.

The continuous development of computers is driven by scientific projects such as the 1,000 Genomes Project or the Large Hadron Collider (LHC) at the CERN European particle-physics lab, by search engines such as Google (see [9.2]), by military supercomputers with petaflop (10^{15}) operations per second [9.3], but also by consumers' demands for increasing computation power, for digital video, digital cameras in cell phones, interactive multimedia, game products, etc., with ever increasing data storage densities and data transfer rates in addition to random access and removability (the ability to separate the media from the drive) [9.4]. In a computer, the memories that directly provide data bits to the microprocessor are semiconductor devices known as the static random access memory (SRAM) and the dynamic random access memory (DRAM). They are fast but need power to maintain the stored bits. When a personal computer (PC) is turned off, the information stored in these memory devices vanishes. The only archival memory in a computer today is a hard disc drive (HDD). Its access time, however, is six orders of magnitude slower than that of SRAM, as seen in the all too familiar wait when a computer is turned on [9.5].

Established by Intel co-founder Gordon Moore in 1965 [9.6], the empirical rule of Moore's law states that the density of transistors on a silicon-based integrated circuit (IC), and so the attainable computing power, doubles about every 18 months, with similar rules for data storage. This had the consequence that the IC components, such as transistors or capacitors, or data bits on HDD shrank to nanometer dimensions so that novel designs and materials concept had to and have to be developed in the future. The rapid development of computers has also initiated novel mathematical techniques. Whereas the computation of a particular equation took more than 2 days in 1980, this only took 10 ms in 2007 (20 million times faster),

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although the computer velocity increased in this period only by a factor of 4,000. This demonstrates that a similar acceleration in computation has been contributed by novel calculation methods [9.7].

Moore's law has held for more than 40 years but there is a sobering consensus in the industry that the miniaturization process or scaling can continue for only another decade or so [9.8]. Therefore, in this section, the present state and future prospects of integrated circuits including strategies beyond complementary metal-oxide-semiconductor (CMOS) technology, of modern lithography technologies, of solid state memory, and of hard disk drives will be discussed. In addition materials (high k, low k) for ultrahigh-density circuit integration will be outlined.

9.1 Transistors and Integrated Circuits

After the invention of the transistor in 1947, the monolithic integrated circuit (IC) was devised in 1958–1959 and in 1971 Intel unveiled the 4004 microprocessor (2,300 transistors) [9.9]. Back in 1993, the Pentium processors with $\sim$ 10 million transistors were released and the current transistor count (see Fig. 9.1) is $\sim$ 4 billion. In 2009 the chip industries had an annual turnover of US$ 212 billion [9.10]. A modern factory costs about US$ 4.5 billion and for a successful operation of this factory an annual output of US$ 7 billion is required [9.10].

The 45 nm technology is available in Penryn processors since November 2007 (P. Otellini, Intel). Prototypes of the 32 nm technology have been manufactured in September 2007 and fabrication started in 2009.

The basic transistor structure in the gate conductors is going to be re-engineered in the current decade. Figure 9.2 shows a transistor structure with a silicon base, a top gate, and a few-monolayer standard SiO_2 (1.2 nm) gate insulator. As the leakage current increases substantially when the insulator is made thinner and thinner, the SiO_2 insulator has to be replaced by a higher-k material (Fig. 9.2, right). Since it is much thicker than the SiO_2 insulator, it has one-hundredth of the leakage current (see Sect. 9.7).

For further scaling, a redesign of the transistor structure, with a very thin conduction channel ($\sim$ 2.0 nm) is suggested (Fig. 9.3, left). The performance of a transistor, which is usually compromised in disordered Si by a high-leakage current due to defect states in the band gap, E_g, is enhanced in nanometer-thin films due to quantum confinement. This gives rise to band edge shifts in both the conduction and the valence bands, and thereby an effective increase of E_g (see [9.11]), which results in an enhanced ratio $I_{ON}/I_{OFF} > 10^{11}$ of the ON and OFF currents, the holy grail of IC designers. Another example is the source-gated transistor (SGT) concept (Fig. 9.3, right), which leads to much less susceptibility to short-channel effects and a higher output independence due to the source barrier being screened from the drain field by the gate (see [9.11]).

The exponential advances in the technologies of complementary metal oxide semiconductor (CMOS) transistors and integrated circuitry predicted by Moore's

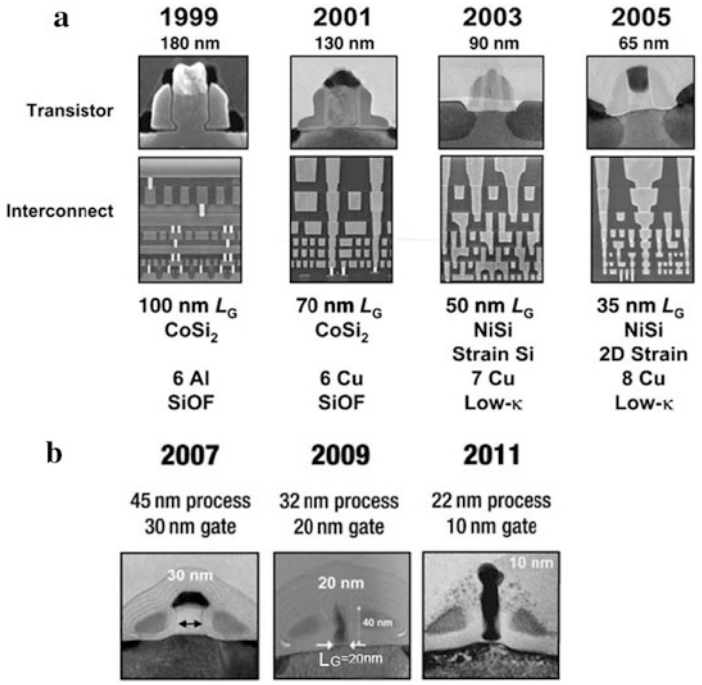

Fig. 9.1 The rate of innovation in transistor density. (**a**) The generations 1999, 2001, 2003, and 2005 with cross sections of the transistors (*upper panels*) and cross sections of the metal interconnects at different magnifications (*lower panels*). L_G is the gate length, "6 Al" means six layers of aluminum, "8 Cu" means eight layers of Cu, etc., $CoSi_2$ or NiSi is the materials of source, drain, and gate electrodes. (**b**) Transistor generations of 2007, 2009, 2011 extending Moore's law. (Reprinted with permission from [9.1]. © 2006 Materials Research Society)

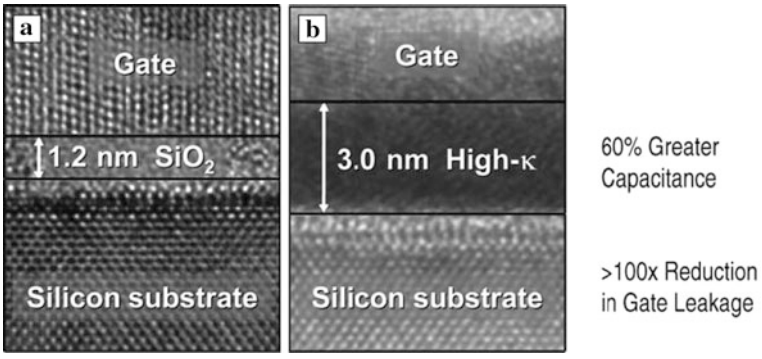

Fig. 9.2 High-resolution cross-sectional images of a transistor structure for SRAMs with a silicon base, a gate on the top, and the dielectric in between. The dielectric layer in (**a**) is a standard SiO_2 gate, 1.2 nm thick. The gate in (**b**) shows a high-*k* dielectric. Although it is much thicker than the gate in (**a**), it has 60% more capacitance and, more importantly, one-hundredth the leakage current because of the thicker gate dielectric. (Reprinted with permission from [9.1]. © 2006 Materials Research Society)

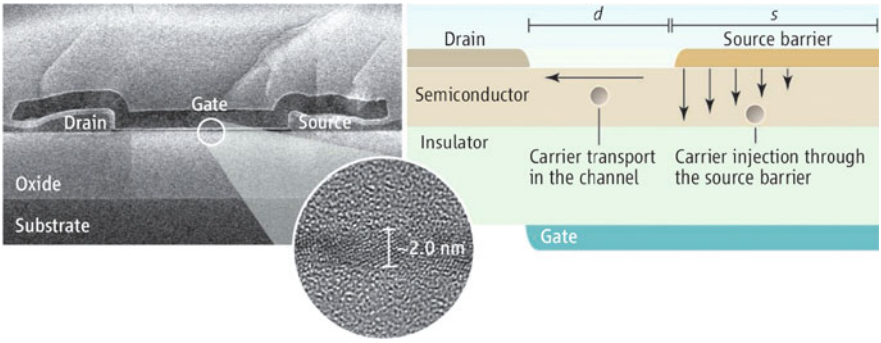

Fig. 9.3 Structure for high-performance transistors in disordered semiconductors. (*Left*) Cross-sectional scanning electron micrograph and transmission electron micrograph of the fabricated nanocrystalline silicon thin film transistors (the minimum channel thickness is 2.0 nm). (*Right*) Schematic of a source-gated transistor (SGT). The arrows in the channel indicate the carrier conduction in the device. (Reprinted with permission from [9.11]. © 2008 AAAS)

law must eventually come to a halt imposed by a hierarchy of physical limits. The five levels of this hierarchy are defined as fundamental, material, device, circuit, and system (see [9.12]). An early analysis of these limitations [9.12] revealed that silicon technology has the potential to achieve a year 2011 terascale integration of more than 1 trillion transistors (with a channel length in the 10 nm range) per chip.

After the termination of the downscaling, conventional transistors could be replaced by a number of devices. One of these could be a silicon-based single-electron transistor (SET; see Fig. 9.4). In a SET, a thin silicon-on-insulator (SOI) may be patterned to form a Si electron island connected to source and drain by two constrictions. The electron island can only be charged at discrete gate voltages and therefore acts as a switch for electrons based on the quantization of electric charge

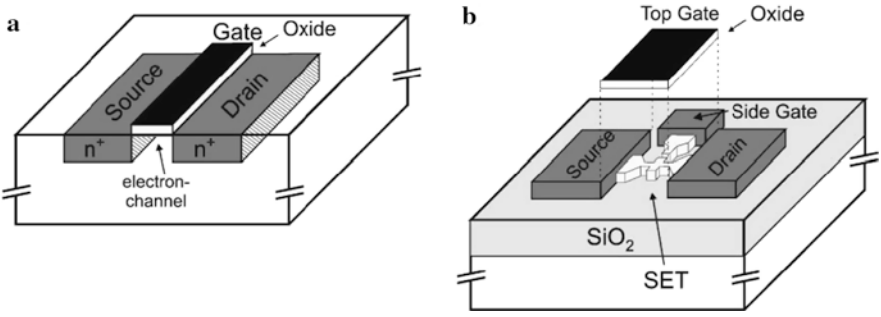

Fig. 9.4 Comparison of (**a**) a MOSFET and (**b**) a silicon-based single-electron transistor. Whereas in the conventional MOSFET a conductive electron channel is formed between two highly doped source and drain regions by applying a gate voltage to a top electrode, the SET uses the charge quantization in a laterally structured electron island which has to be fabricated out of a silicon-insulator film. (Reprinted with permission from [9.13]. © 2001 Elsevier)

(see Sect. 1.3) rather than on the charging of a capacitor like in a metal oxide–semiconductor field-effect transistor (MOSFET). The outstanding property of SETs is to switch the device by adding only one electron to the gate whereas common MOSFETs need about 10^3–10^4 electrons. In addition, the switching times are short because of the low RC time constants of the small constrictions. First SETs working at ambient temperature have been demonstrated earlier [9.14, 9.15]. Carbon nanotube electronics is another approach with a remarkable pace of advances. The first nanotube-based transistor appeared in 1998 [9.16]. Logic circuits [9.17] as, e.g., an inverter (NOT gate) (see Fig. 9.5) or a ring oscillator [9.18], build from nanotube transistors appeared in 2001. In 2006 a five-stage, ten-transistor ring oscillator built as an IC on a single nanotube [9.20] was demonstrated. As a further step for building reliable devices it was shown that carbon nanotubes can be sorted out by both diameter and electronic type (metallic or semiconducting) [9.21].

Graphene nanoribbons with sub-10 nm width were theoretically predicted to be semiconducting (see [9.22]), as demonstrated experimentally [9.22]. Graphene nanoribbon field-effect transistors (GNRFETs; see Fig. 9.6) were demonstrated with I_{ON}/I_{OFF} ratios up to 10^6, an on-state current density as high as $\sim$ 2,000 μA/μm, a carrier mobility of $\sim$ 200 cm^2/Vs, and a scattering mean free path of $\sim$ 10 nm [9.22]. Scattering by edges, acoustic phonons, and defects may play a role [9.22]. The sub-10 nm GNRFETs are comparable to small diameter ($d \leq 1.2$ nm) carbon nanotube FETs with Pd contacts in on-state current density and I_{ON}/I_{OFF} ratio, but have the advantage of producing all-semiconducting devices [9.22].

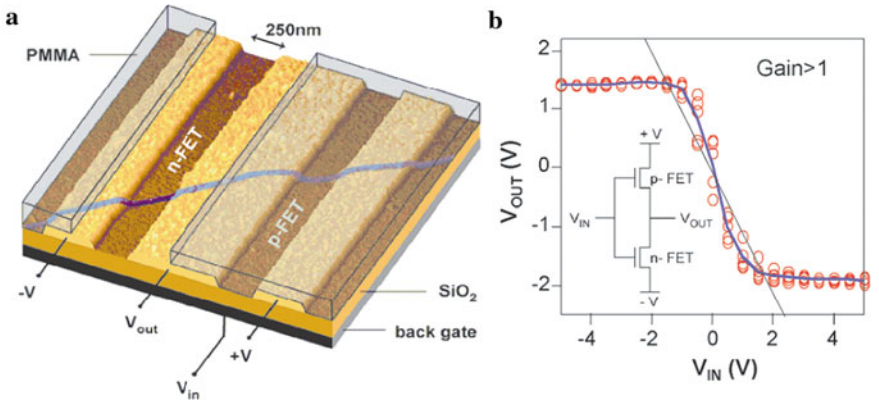

Fig. 9.5 Atomic force microscope (AFM) image showing the design of an intramolecular logic gate. A single-nanotube bundle is positioned over the gold electrodes to produce two p-type CNTFETs (carbon nanotube field-effect transistor) in series. The device is covered by poly(methyl methacrylate) (PMMA) and a window is opened by e-beam lithography to expose part of the nanotube. Potassium is then evaporated through this window to produce a n-CNTFET, while the other CNTFET remains p-type. (**b**) Characteristics of the resulting intramolecular voltage inverter. Open *red circles* are measuring data and the *blue line* is the average of these data. The thin straight line corresponds to an input/output gain of one. (Reprinted with permission from [9.19]. © 2004 Materials Research Society)

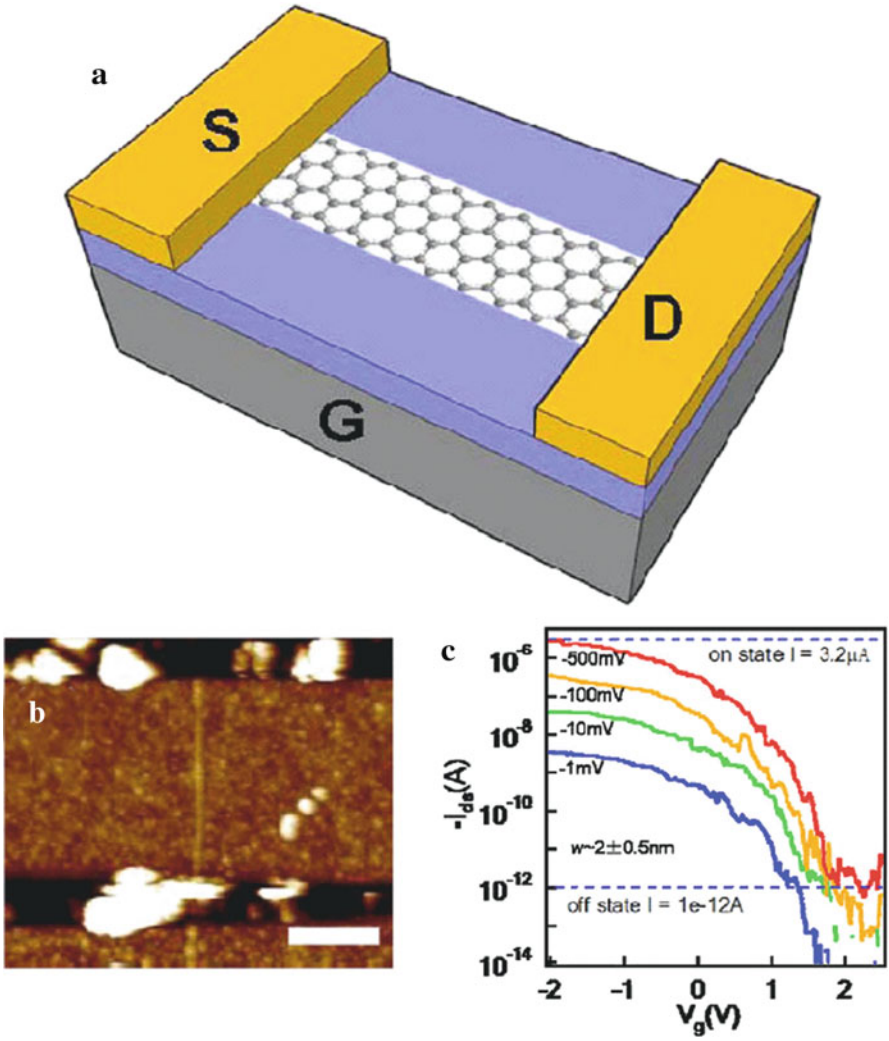

Fig. 9.6 The graphene nanoribbon field-effect transistor (GNRFET). (**a**) Schematics of GNRFET on 10 nm SiO_2 with Pd source-drain electrodes. $P^{++}Si$ is used as backgate. (**b**) Atomic force microscope (AFM) image of a GNRFET with a width of $\omega \sim 2 \pm 0.5$ nm and a length of $L \sim 236$ nm. Scale bar is 100 nm. (**c**) Transistor performance of the GNRFET in (**b**) with current versus gate voltage $I_{ds} - V_{gs}$ under various V_{ds} and an I_{ON}/I_{OFF} ratio of $> 10^6$ achieved at room temperature. (Reprinted with permission from [9.22]. © 2008 American Physical Society)

High-speed integrated circuits may find many new applications when they could be printed with inks containing high-performance semiconducting materials. In inks with a dispersion of single-walled carbon nanotubes the conductivity of the metallic nanotubes can be suppressed by attaching fluorinated olefins which depletes the density of states at the Fermi level [9.23]. Transistors manufactured using this ink

show a high mobility of 100 cm^2 $(Vs)^{-1}$ *and* an on/off ratio as high as 10^5. Thin-film transistors can be printed with a spatial resolution of 1 μm or less by inkjet printing. Since individual nanotubes have mobilities of 10,000 cm^2 $(Vs)^{-1}$ and more, it is possible that a mobility superior to that of single-crystal silicon (1,000 cm^2 $(Vs)^{-1}$) can be achieved.

9.2 Extreme Ultraviolet (EUV) Lithography – The Future Technology of Chip Fabrication

Extreme ultraviolet lithography (EUVL; see [9.24]) appears to be the most promising fabrication technology for future computer chips [9.25]. With the first-generation ASML demotools for 13.5 nm EUVL scanners deployed in 2006 (see Fig. 9.7b), the first 45 nm logic test chips with functional transistors were fabricated [9.27] with properties consistent with those printed by a standard 193 nm immersion process. With the ASML EUV "preproduction tool" available in 2009, this development will be continued for a test fabrication of 22 nm structural sizes, so that in 2011 EUV lithography will be the most likely technical option for the production of computer chips (see Fig. 9.7a).

For the reduction of the structural sizes in computer chips, the minimum half-pitch (HP; see Sect. 3.10) or the

$$\text{resolution} = k_1 \cdot \lambda/\text{NA}$$

of the optical production tools is of particular importance. According to this relationship the resolution can be improved by reducing the wavelength λ of the light for imaging, by increasing the numerical aperture NA of the optical system, and by reducing the process parameter k_1 which characterizes the printing of a pattern on the mask. Small k_1 values can only be achieved by complex and costly production processes. For $k_1 < 0.25$, dense structures cannot be printed in a single-illumination process but multiple illumination is required (double patterning, spacing [9.28]). A decreased λ and an increase of NA can enhance the resolution, independent of k_1.

In the production of computer chips with 193 nm wave length ArF lasers, where the maximum NA = 1.35 is already approached, the production of structures 32 nm wide (32 nm logic node) in the near future requires the lowering of k_1 to below 0.25 which makes the mask cost escalate. That means that only the lowering of λ to EUV can provide long-term solutions with good prospects, also beyond the 22 nm node.

For EUV lithography novel techniques had to be developed. For powerful radiation sources with several hundreds of watts in the 13.5 nm wavelength regime (Fig. 9.8a) plasmas of Sn or Xe, generated by laser focusing or discharge, are employed. For the manipulation of the 13.5 nm wavelength radiation no lenses but only multilayer interference mirrors (see Sect. 4.3.6) can be used, where Mo–Si multilayers with a layer thickness of λ/4 = 3–4 nm exhibit a high reflectivity (Fig. 9.8a) when fabricated with 150 pm shape and positioning precision [9.25]. This precision

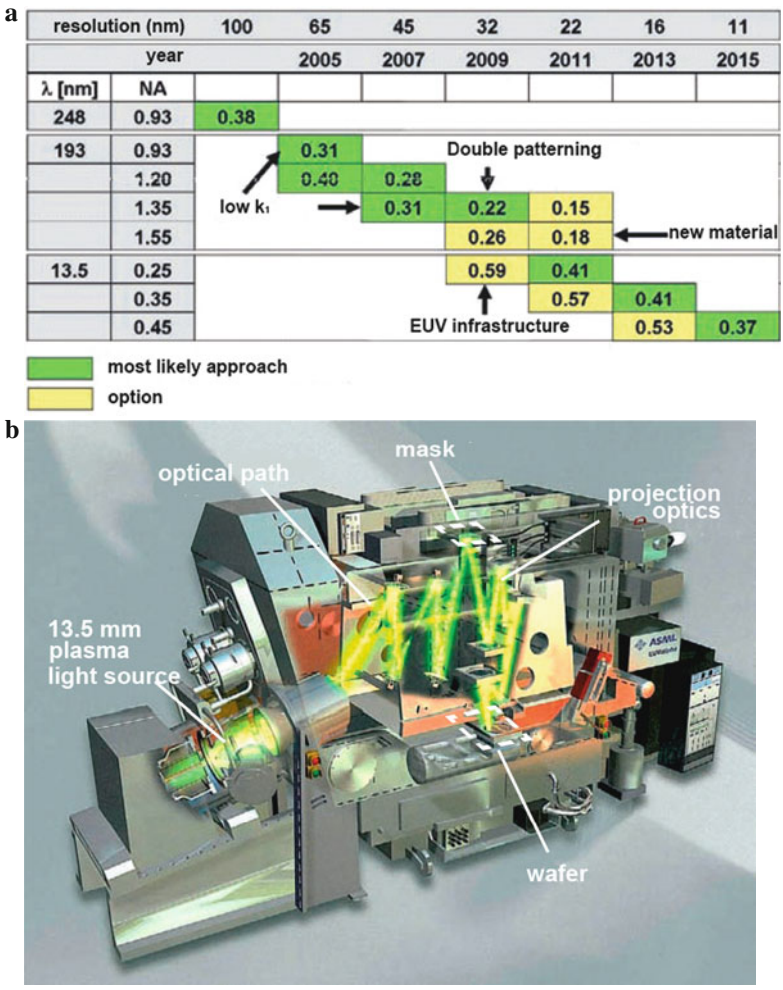

Fig. 9.7 (**a**) The ASML/Carl Zeiss SMT roadmap indicates which technological option – conventional 193 nm lithography or 13.5 nm EUV lithography – will most likely be employed at which time in order to meet the requirements of a particular resolution. The comments indicate the outstanding challenges. (**b**) ASML EUV wafer scanner with the optical system by Carl Zeiss STM [9.26]. The 13.5 nm EUV irradiation generated by a plasma source illuminates the mask and the projection optics image the mask unto the wafer [9.25]. (Reprinted with permission from [9.26] and [9.25]. © 2008 Photonik; T. Heil and M. Lowisch, Zeiss, ASML)

is equivalent to a 2 mm high hill on a 1,000 km distance. The mask with a similar multilayer structure as the mirrors is operated in reflection. The mask patterns are written on the surface of this multilayer where they suppress reflection. Corrections have to be applied to the chip mask to compensate for flare, i.e., variations in the power spectral density of the optical path differences, and of the mask shadowing

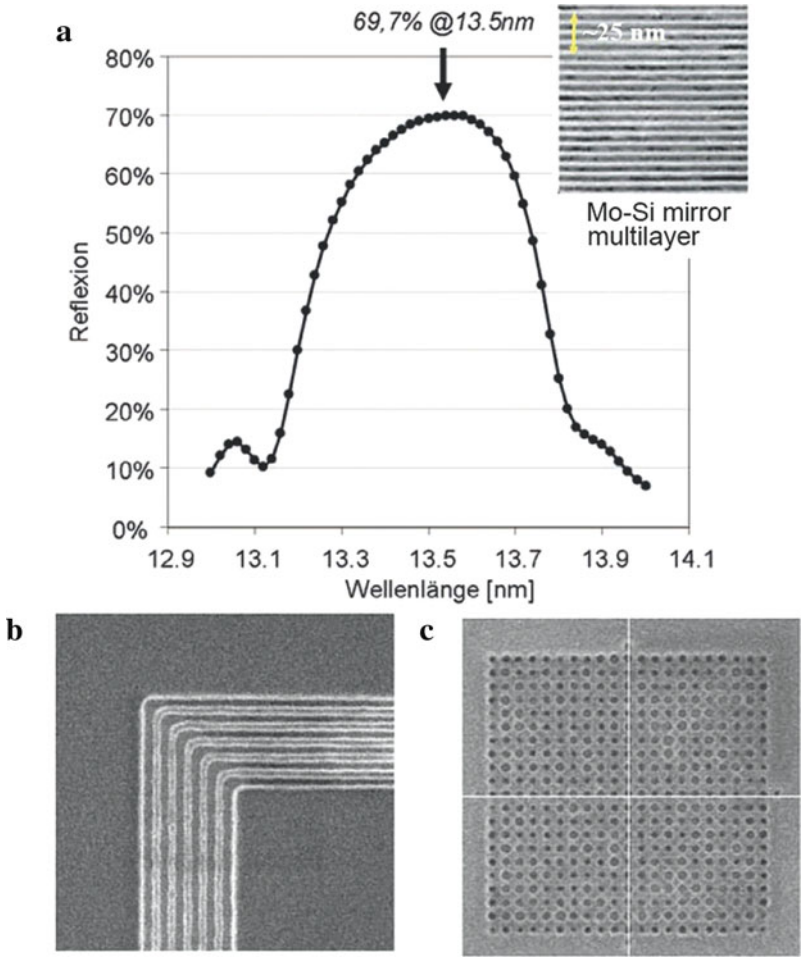

Fig. 9.8 (**a**) Reflection spectrum of a Mo–Si mirror multilayer. The inset shows a transmission electron micrograph of the Mo–Si multilayer. (**b**, **c**) Scanning electron micrograph of 35 nm wide conduction lines (**b**) and 32 nm diameter contact points (**c**) generated by EUV lithography. (Reprinted with permission from [9.25]. © 2008 Photonik; T. Heil and M. Lowisch, Zeiss.)

effects due to a non-normal illumination of the mask plane [9.27]. The projection optics have to image the mask structures without defects over the width of 26 mm of the chip onto the wafer, which is covered with a high-sensitivity resist [9.29], in a time-saving single scan. Since the width of the single nanostructures on the chip differs from the total chip size by 6 orders of magnitude, the information contents of 10^{12} pixels – corresponding to a HDTV image of the size of 1 km^2 – can be transferred to the wafer in a single illumination. This may demonstrate the enormous productivity of the EUV technology. In Fig. 9.8b, c structures generated by means of EUV lithography are shown.

9.3 Flash Memory

Flash memory relies for data storage on controlling electrons stored in a transistor's gate circuit [9.30–9.32]. Floating gate flash memory is a fast growing memory segment [9.30], driven by the rapid growth of portable devices such as digital cameras and cell phones. The technology allows for data stored in multiple memory cells to be erased in a single action (a "flash") by means of an applied voltage. Flash memory cells have been scaled down to 32 nm half-pitch with a cell size of 0.0112 μm^2 and a word line spacing of 20 nm where, however, crosstalk becomes an issue [9.33]. Flash data storage devices with 3 gigabytes per cm^2 [9.34] have been achieved. For further decreasing size, the scaling constraints will require new materials, [9.32] and novel concepts such as charge storage in nanocrystals [9.35] in a non-conducting floating node, which replaces the normally conducting floating gate, or organic flash memory devices based on alterations of a polymer's conformation [9.36]. A conventional floating gate non-volatile flash memory cell (Fig. 9.9) contains a metal oxide semiconductor (MOS) transistor with two gates, a floating gate and a control gate. The memory cell consists of an *n*-channel transistor with the addition of an electrically isolated polysilicon. Any charge present on the floating gate is retained due to the inherent Si–SiO_2 energy barrier height, leading to the non-volatile nature of the memory cell. Characteristic of the structure is a thin tunneling oxide (~10 nm), an oxide-nitride-oxide (ONO) interpoly dielectric (IPD) that resides between the two polysilicon gates, and a short electrical channel length. The threshold voltage of the device can be changed by modifying the charge on the floating gate, which can retain this charge for many years. Data can be stored in the memory by adding or removing charge.

Programming of a flash cell can be performed with channel electrons of high kinetic energy – so called hot electrons – which can surmount the 3.2 eV Si–SiO_2 energy barrier. When these electrons experience a collision with the Si lattice, they

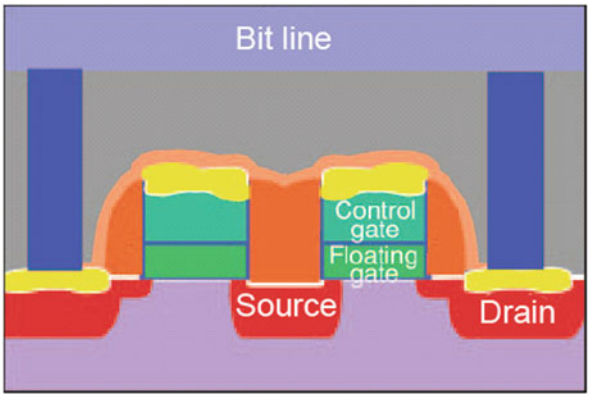

Fig. 9.9 Flash memory cell: cross section along the channel. (Reprinted with permission from [9.30]. © 2004 Materials Research Society)

are directed toward the Si–SiO_2 interface with the aid of the gate field. The electron is subsequently captured on the floating gate and retained as stored charge. The electrical *erasure* of flash memory is achieved by electron tunneling in a high field (8–10 MV/cm) between the floating gate and the channel. When the erase operation has been completed, electrons have been removed from the floating gate, reducing the cell threshold. While programming is selective to each individual cell, erasing is not, with many cells (typically, 64 kbytes) being erased simultaneously [9.30].

Scaling limitations of the flash memory will emerge below the 70 nm lithography node due to the inability of a shorter channel length to withstand the required programming voltage. By choosing dielectric alternatives to SiO_2, the barrier can be tailored to allow hot electron injection to occur at lower voltages. Scaling also affects the adequate coupling of the control gate to the floating gate by the IPD, while minimizing any leakage through the dielectric. An alternative may be to replace the IPD with higher-dielectric constant (high k) materials compared to SiO_2. One thrust to overcome the limitations of the scaling of flash memory is electron storage in nanocrystals in a non-conducting floating node, instead of the conventional conducting floating gate. In Fig. 9.10 3 nm HfO_2 nanodots with densities of 6×10^{12} cm^{-2} in a SiO_2 film on a Si substrate are shown. Memory cells with HfO_2 nanodots can be erased in 0.1–1 ms and exhibit retention times of 10^8 s (>3 years). They are considered suitable as charge storage nodes in future 45 and 32 nm generations [9.35].

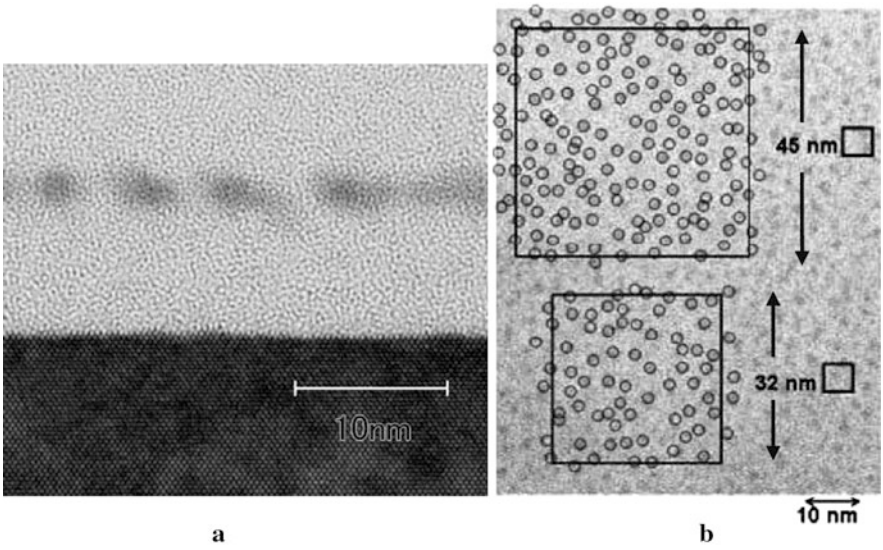

Fig. 9.10 (**a**) Cross-sectional and (**b**) plane-view transmission electron micrographs of ultrahigh-density HfO_2 nanodots in SiO_2 on a Si substrate. The thickness of the initially deposited HfO_2 film was 0.5 nm. In (**b**), nanodots are marked with open circles for clarity. The dimensions of the gate areas of the future 45 nm and the 32 nm technology nodes are also shown. (Reprinted with permission from [9.35]. © 2006 Japan Society of Applied Physics)

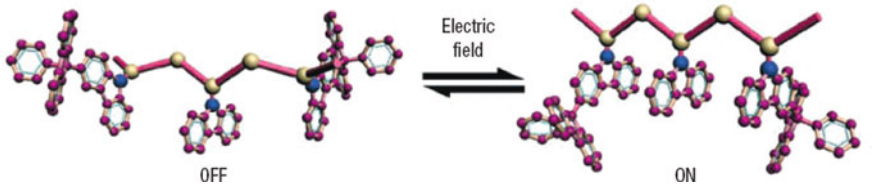

Fig. 9.11 Schematic diagram for the switching transition of the poly(*N*-vinylcarbazole)-phenylfluorene (PVK-PF) molecule from the low conductivity to the high-conductivity states. (Reprinted with permission from [9.36]. © 2008 Nature Publishing Group)

Another choice for scalable flash memories could be organic semiconductor polymers which transport charge via their π orbitals, the orientation of which depends on the conformation of the polymer and affects the charge mobility. The first organic non-volatile flash memory devices were designed [9.36] by taking poly(*N*-vinylcarbazole) (PVK), which transports charge via intrachain stacked π orbitals that result from face-to-face conformation of the carbazole (Cz) group (Fig. 9.11). By adding to PVK the bulky phenylfluorene (PF) as a side group, the steric effects were used to tune the conformation of the polymer. When applying a voltage of 2.2 V to a PVK-PF sandwich device, a sharp increase of the current was observed – the ON state ("write" process) with Cz stacked face to face. The application of a reverse voltage induces conformational changes of the PF groups to the initial state, blocking the face-to-face orientation of Cz – the OFF state (Fig. 9.11). An ON/OFF current ratio of $>10^4$ has been obtained and no degradation was observed of the OFF and ON states after 10^8 read cycles at –1 V [9.36]. Experts see flash and random-access memory (RAM) technologies reaching scale limitations in a similar time-frame after 2010 [9.31]. A new non-volatile technology – phase-change random access memory (RAM) or PRAM – is viewed as the most promising among alternatives to flash. In PRAM (see below), data are stored by altering the chip material's atomic structure, obtaining improved data density and other benefits over standard flash [9.31].

9.4 Emerging Solid State Memory Technologies

Currently, there are three commercially available families of memory: dynamic random access memory (DRAM), static random access memory (SRAM), and flash memory. Consumer products typically use combinations of these three memory families, each having their unique advantages: DRAM is cheap, SRAM is fast, and flash is non-volatile (see [9.37]). In the semiconductor industry, increasing miniaturization is beginning to place strains on existing technologies for data storage and computer memory, which could soon reach fundamental physical limitations. In addition, there is a need to develop new memory technologies that can provide low-power operation and low standby battery drain. These trends have accelerated

Table 9.1 Performance characteristics of conventional and emerging memory technologies. SRAM – static random access memory; DRAM – dynamic random access memory; Flash – flash memory; PRAM – phase change memory; MRAM – magnetoresistive memory; FeRAM – ferroelectric memory; NRAM – nanotube random access memory. The NRAM data should be considered as a target established by Nantero, Inc. [9.37]

	Conventional technologies			Emerging technologies			Prototypes
Parameter	SRAM	DRAM	Flash	PRAM	MRAM	FeRAM	NRAM
Read speed	Fastest	Medium	Fast	Fast	Fast	Fast	Fast
Write speed	Fastest	Medium	Slow	Fast	Fast	Med.	Fast
Cell density	Low	High	Medium	High	High	Med.	High
Process technology, nm	130	80	56	90	130	130	22
Nonvolatility	No	No	Yes	Yes	Yes	Yes	Yes
Future scalability	Good	Limited	Limited	Exell.	Good	Limited	Scalable

the development efforts in universal memory products that integrate the best features of existing memory types into a single package. The new universal memory chip should be cheap and compact with the density of DRAM, draw and dissipate little power, switch in nanoseconds and should be compatible with CMOS architectures [9.38]. There are several possible candidates for a universal memory that are being actively explored by the industry. The new technologies that have already found a niche in the memory market include phase-change memory (PRAM), magnetoresistive RAM (MRAM), and ferroelectric RAM (FeRAM). A number of other technologies including resistance RAM (ReRAM), carbon nanotube RAM (NRAM), and race track memory (RM), which will be briefly discussed below, are being developed to compete in non-volatility with flash memory and in speed and density with conventional SRAM and DRAM [9.37].

Although existing memory technologies continue to advance, providing faster, smaller, and cheaper memory, they are not expected to scale down beyond a very few additional process technology nodes. The most widely used commercial nonvolatile memory – flash – has a low write speed leading to a slow random access. New emerging memory technologies such as FeRAM, MRAM, and PRAM are currently in use in a number of applications where the limitations of flash are an issue. A comparison of the performance characteristics of conventional and novel advanced memory technologies including carbon-nanotube-based (NRAM) prototypes is given in Table 9.1.

9.4.1 Phase-Change Memory Technology

Phase-change non-volatile semiconductor memory technology is based on an electrically initiated, reversible rapid amorphous-to-crystalline phase-change process in multicomponent chalcogenide alloy materials similar to those used in rewritable optical disks (see Sect. 9.6) [9.39, 9.40]. Long cycle life, low programming energy,

and excellent scaling characteristics are advantages that make phase-change semiconductor memory (PCM) a promising candidate [9.41, 9.42] to replace flash memory in future applications [9.39], [9.43]. Under R&D scrutiny for years, Intel Corp. and STMicroelectronics announced in February 2008 the shipment of a 128 Mb device codenamed "Alverstone" using PCM technology, fabricated on a 90 nm process. This may bring PCM technology one step closer to adoption (see [9.43]).

A schematic cross section of a phase-change memory cell together with the corresponding current–voltage curves is shown in Fig. 9.12. The cell is a nonlinear resistor and the readout is performed at low bias (READ in Fig. 9.12b), where the low-field resistance changes by orders of magnitude depending whether the Ge–Sb–Te chalcogenide semiconductor material in the active region of the device is crystalline or amorphous. The propensity to amorphize is due to the chalcogenide (Group VI) components such as Te, which are good glass formers because of their two-fold-coordinating chemical bonds that can produce linear, tangled polymer-like clusters in the melt. This increases the viscosity of the liquid, inhibiting the atomic motion necessary for crystallization (see [9.39]). To reach the switching regions (SET for crystallization and RESET for amorphization due to subsequent quenching, see Fig. 9.12b), the bias is raised above the switching voltage so that enough current can flow through the cell, heating up the active region (Fig. 9.12a) and resulting in either the amorphous–crystalline phase change to the SET state (programming) within <20 ns (see [9.39]) or the crystalline–amorphous phase change to the RESET state at higher temperatures within a few nanoseconds (see [9.39]) with subsequent quenching-in of the amorphous state.

The crucial problem for electronic phase-change data storage is understanding electronic transport which is different in the crystalline and amorphous phases (see [9.40]). While the resistivity in the crystalline phase exhibits an ohmic behavior the

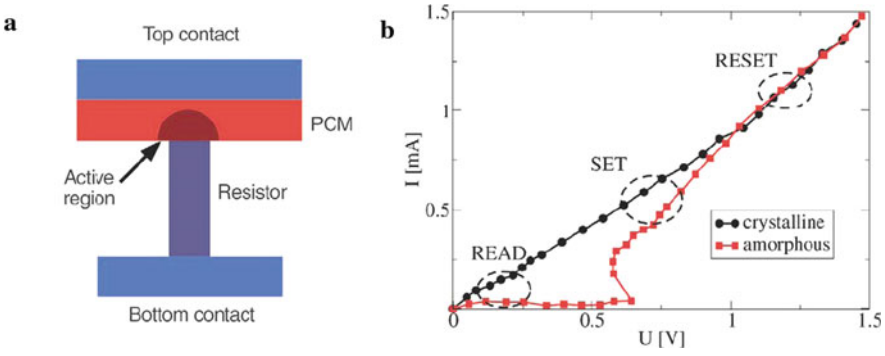

Fig. 9.12 (**a**) Schematic of a phase change memory cell. Depending on the state of the active region (crystalline or amorphous), the resistance of the cell changes by several orders of magnitude. (**b**) Current–voltage curve for a phase-change memory cell. SET and RESET denote the switching regions, while READ denotes the region of readout [9.40, 9.44]. (Reprinted with permission from [9.40]. © 2008 Materials Research Society)

amorphous phase shows threshold switching, allowing the phase transition to occur at modest voltages. The current which is low at small electric fields, increases dramatically when a critical electrical field is exceeded. This leads to a high current in the amorphous phase, generating significant heating which gives rise to the desired phase transition. In modeling of the threshold behavior, at zero electrical field V_A an electron trapped in the amorphous structure needs to overcome the energy barrier E_C–E_T in order to hop onto the neighboring trap, where E_C and E_T are the energies of the conduction band edge and of the trap state, respectively. The application of a sub-threshold voltage changes the shape and the height of the barrier, and therefore the activation energy for electron transport, leading to the generation of carriers and a current

$$I = 2qAN_T \frac{\Delta z}{\tau_0} \exp\left[(E_F - E_C)/kT\right] \sinh\left(\frac{qV_A \Delta z}{kT2u_a}\right)$$

exponentially rising as a function of voltage. Here A is the area of the contact, N_T the integral of the trap distribution, Δz the intertrap distance, τ_0 the escape time for a trapped electron, E_F the Fermi energy, q the elementary charge, and u_a the thickness of the amorphous chalcogenide. This relation correctly reproduces the current–voltage characteristics of the sub-threshold regime. At large electric fields, the equilibrium distribution of electrons in sub-threshold traps is suggested [9.45] to change into a non-equilibrium distribution at which electrons acquire an effective temperature. As a result of this electron heating, charge carriers from deep traps are allowed to access shallow trap states at higher energies closer to the conduction band edge via thermal emission or tunneling. Because of the exponentially rising emission and the finite relaxation time of the trapped carriers, the occupation of the shallow traps increases with increasing voltage, moving the electron distribution from the equilibrium Fermi distribution to a non-equilibrium distribution. This causes the conductivity to increase exponentially, which leads to a steep enhancement of the current in the system.

Crystallization kinetics is the time-limiting step in the application of phase-change materials. Since an atomistic understanding of these kinetics is missing, experimental studies have focused to the determination of activation barriers for the overall crystallization process, making use of Johnson–Mehl–Avrami concepts (see [9.40]). More recently, the contributions of nucleation and crystal growth to crystallization have been separated, being facilitated by the substantial density change between the amorphous and crystalline phases of 5–10% [9.46]. From atomic force microscopy studies the temperature dependences of nucleation and crystal growth with the corresponding activation energies were determined in dependence of composition. The ratio T_G/T_M of a phase-change material, where T_G is the glass transition temperature and T_M the melting temperature, obviously can provide a first approach to predict the crystallization mechanism: within the interval $0.5 \leq T_G/T_M \leq 0.55$, the materials with lower T_G/T_M values show nucleation-dominated crystallization while materials with values at the upper limit are characterized by growth-dominated crystallization (see [9.40]).

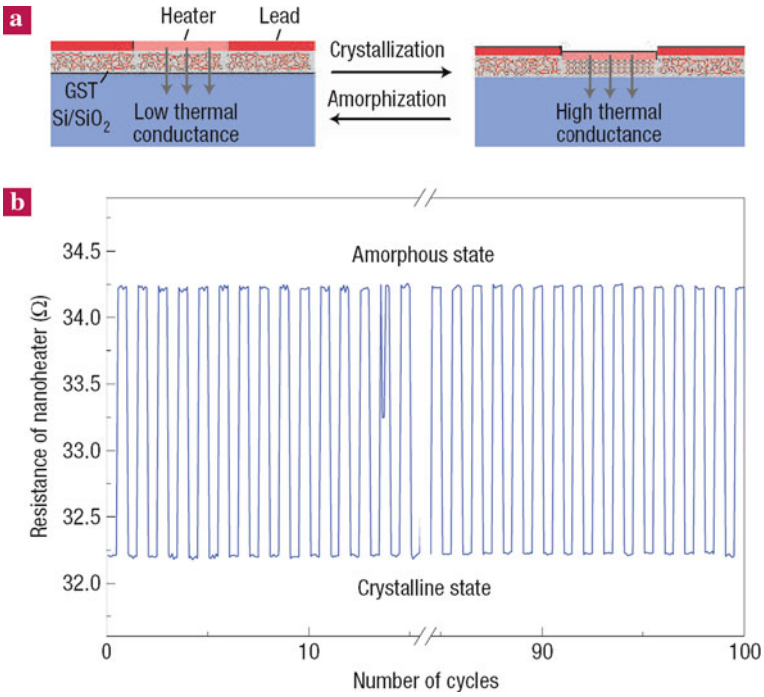

Fig. 9.13 An all-thermal phase-change memory concept. (**a**) Illustration of the concept. By applying the appropriate current (heat) pulse the $Ge_2Sb_2T_5$ film is written (amorphized) and erased (crystallized) by a nanoheater. The phase of the film is read at lower currents by sensing the thermal resistance of the heater, which depends on the phase of the $Ge_2Sb_2Te_5$ film underneath the heater. (**b**) A portion of 100 cycles of successful amorphizing and crystallizing using the all-thermal memory cell. (Reprinted with permission from [9.47]. © 2006 Nature Publishing Group)

An all-thermal phase-change memory concept has been presented (Fig. 9.13) by using a nanoheater, which can be fabricated with a size less than 50 nm, for reversible phase-change recording and reading. Because the amorphous phase has a lower thermal conductivity, the resulting temperature of the substrate and thus the resistance of the platinum heater is higher than in the crystalline phase for a given bias current. The amorphization and crystallization kinetics can, in principle, be as fast as 8 GHz for dimensions smaller than 50 nm (see [9.47]). Another promising approach for optimizing the performance of phase-change electronic memories is the use of nanostructures. Phase change nanostructures were prepared by filling prepatterned holes with a GeSbTe alloy [9.48] or by self-assembling sublithographic GeSbTe nanowires to construct a phase-change device with a threshold voltage of 1.8 V [9.38].

The endurance of phase-change memory cells has been reported as being between 10^9 and 10^{13} write/erase cycles – considerably in excess of nominal 10^6 cycle endurance of flash memory. Data retention and life times of 10 years at

110°C have been anticipated (see [9.39]). One of the strongest advantages of phase-change memory cells is that no physical limit to scaling has been identified for the next lithography generations. Nevertheless, a number of challenges remain before the potential of phase-change memories can realized in high-density commercial products [9.39]. The identification of extremely fast phase-change materials would help to produce a memory that combines the attractive features of the two existing memory technologies, namely the non-volatility of flash memory and the speed of dynamic random access memory (DRAM). This would provide a truly universal memory [9.40]. The threshold switching of phase change materials has been modeled numerically [9.49].

9.4.2 Magnetoresistive Random-Access Memories (MRAM)

The magnetic random-access memory (MRAM) making use of magnetic tunnel junctions (see Sect. 1.4) can provide a non-volatile memory with the density of DRAM (dynamic random-access memory), the speed of SRAM (static random-access memory), unlimited write cycles, and significantly lower write-power requirements than flash memory (commonly used in USB sticks, digital cameras and cell phones) [9.50]. MRAM could be the "dream memory" since it has the potential to replace all the existing memory devices in a computer. This "universal" memory then could become an enabling technology for integrating a computer on a single chip [9.5]. In a magnetic tunnel junction (MTJ), which is the building block of the MRAM, two ferromagnetic layers are separated by a thin (1.2 nm) insulating layer, giving a much larger change in resistance (∼60%; see Fig. 9.14c) from the parallel to the antiparallel magnetization states than a GMR device. The sense and write lines of a magnetic tunnel junction are shown in Fig. 9.14a together with the detailed structure of the MTJ in Fig. 9.14b. A recent development, already in use by Freescale Comp., a former spin-out of Motorola and IBM, is the "toggle" switching of the magnetization in the free layer (see Fig. 9.15) by which switching errors can be suppressed. The synthetic antiferromagnet (SAF) with toggle switching provides another benefit for scaling, because the magnetic anisotropy of the composite structure can be more easily controlled than that of a single layer in order to maintain the anisotropy energy of the shrinking bit by a factor of 30–50 larger than kT.

Magnetic tunnel junctions with much higher magnetoresistive ratios (∼ 350%) were theoretically predicted for Fe/MgO/Fe sandwiches oriented in the (100) direction [9.53] and demonstrated experimentally [9.54, 9.55] (see Fig. 9.16) with tunneling magnetoresistance ratios of more than 400% (see [9.57]). This shows that not exclusively the nature of the ferromagnetic electrodes but the chemical bonds formed at the ferromagnet/insulator interface influence the magnitude of the tunneling current as described in terms of a tunneling current matrix element. The tunneling current is proportional to the density of states multiplied by the corresponding tunneling matrix element, which will be strongly influenced by the conduction band wave functions in the ferromagnet. Since the electronic wave

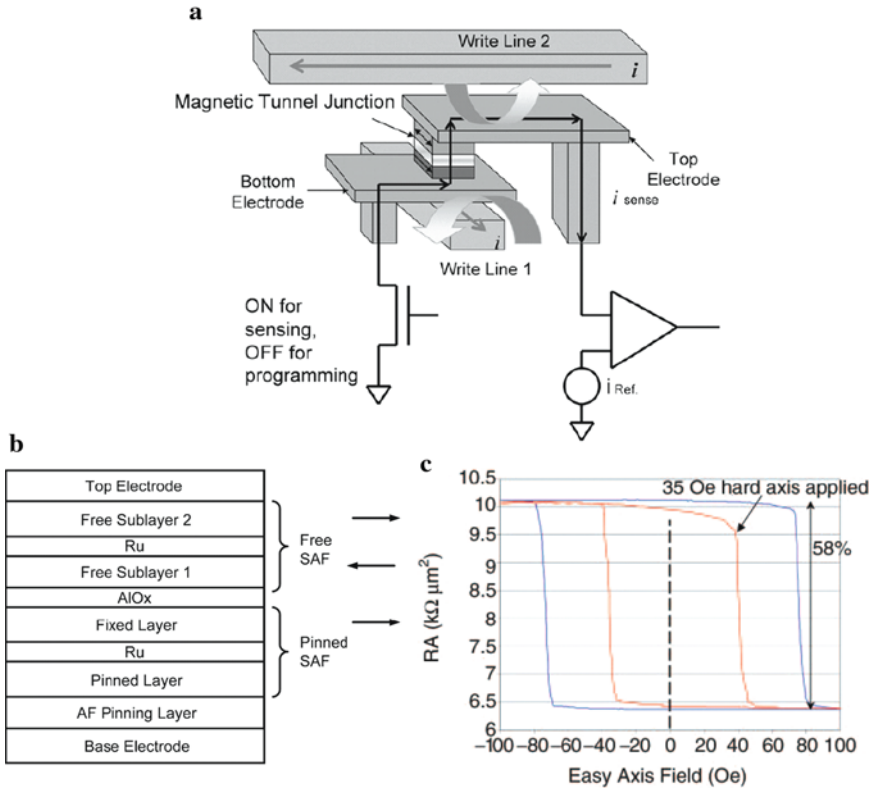

Fig. 9.14 (**a**) MRAM (magnetoresistive random-access memory) bit cell structure, showing the sense path and programming lines. (**b**) Bit cell material stack of a magnetic tunnel junction (MTJ) showing the synthetic antiferromagnetic (SAF) free layer [9.51]. (**c**) Resistance (expressed as resistance-area product RA of the MTJ material) versus field for a 0.6 μm × 1.2 μm bit with (*red curve*) and without (*blue curve*) hard axis field applied. The parallel magnetization is low resistance and the antiparallel state is high resistance with a ratio in this case of 58% [9.52]. (Reprinted with permission from [9.51] (**a**) (**b**) and [9.52] (**c**). © 2005 IEEE (**a**) (**b**) and © 2004 Materials Research Society (**c**))

functions decay into the tunnel barrier depending on the symmetry of the wave function, states with a more delocalized character will decay less quickly into the barrier and, therefore, have a correspondingly larger matrix element. This means that the majority and minority spin-polarized conduction band states in the ferromagnet, with significantly different symmetries, will decay at different rates across the tunnel barrier, leading to an increased (or decreased) spin polarization of the tunneling current. Thus the tunneling barrier can act as a spin filter, giving rise to a resistivity strongly dependent on the mutual orientations of magnetizations in the magnetic tunneling junction.

Further scaling of MRAM is expected from nanoscale current-induced magnetization reversal by spin torque (see Sect. 8.7) in trilayer GMR structures [9.50].

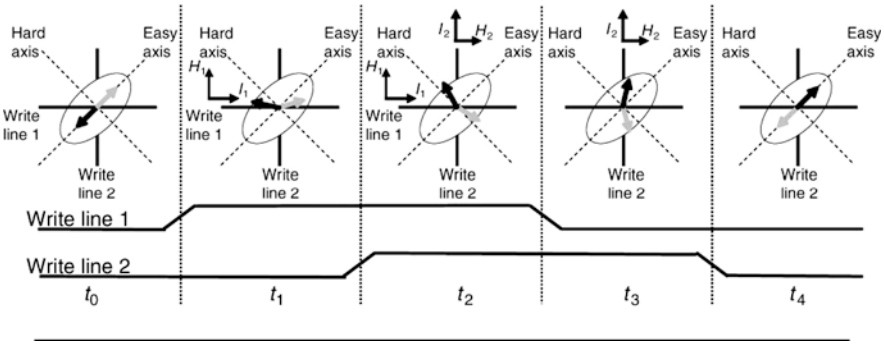

Fig. 9.15 The pulse sequence for toggling a magnetic tunnel junction MRAM bit. The pulses of the two write lines rotate the synthetic antiferromagnet (SAF) by 180° to switch between the antiparallel (high resistance) and parallel (low resistance) orientation of the magnetization. Only the bottom layer of the SAF, close to the insulating layer, determines the resistance of the bit. I_1 and I_2 are the programming currents in the lines 1 and 2, respectively, whereas H_1 and H_2 are the corresponding magnetic fields. Timing intervals between pulses are indicated by t_1, t_2, t_3, t_4. (Reprinted with permission from [9.52]. © 2004 Materials Research Society)

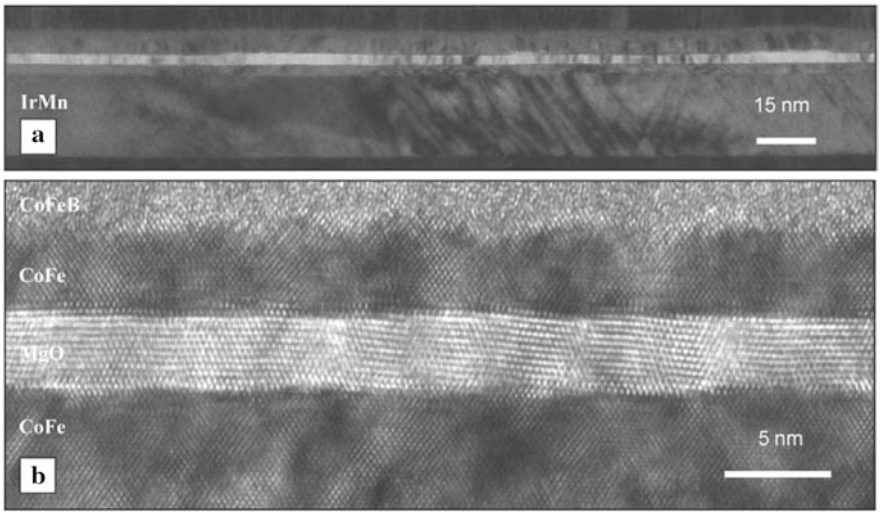

Fig. 9.16 Transmission electron micrographs of a magnetic tunnel junction showing a highly oriented (100) MgO tunnel barrier. (**a**) Growth of ultrasmooth underlayers formed from TaN, Ta, the antiferromagnetic exchange-bias layer of $Ir_{76}Mn_{24}$, the ferromagnetic reference layer, the MgO layer with the subsequent counter ferromagnetic electrode of amorphous $[Co_{70}Fe_{30}]_{80}B_{20}$. (**b**) High-resolution image along the [9.110] zone axis showing atomically resolved lattice planes with (100) planes perpendicular to the growth direction. (Reprinted with permission from [9.56]. © 2006 Materials Research Society)

This development is key for scaling MRAM to at least the 32 nm lithography node. The requirement for this novel spin momentum transfer (SMT) effect is that the dimensions of the bit must be well under 100 nm. This innovation will significantly shrink the size of the bit and allow the bit to be switched at much lower energy than the "toggle" bit [9.50]. The key features of future MRAMs incorporating SMT switching are compiled in Table 9.2. Future SMT MRAMs may outperform volatile DRAMs and SRAMs or flash memories which exhibit long program times, limited write ability, and high-power consumption.

For current-induced spin torque in an MTJ, the tunneling current arriving at the storage layer is spin-polarized because the population of the tunneling electrons with one sign of spin is higher than with the other sign (see [9.57]). The net spin moment of the tunneling current is proportional to both the degree of polarization and the current density, and can generate a torque, on the local magnetization. Depending on the direction of the tunneling current, the spin torque switches the storage layer magnetization to a state either parallel or antiparallel to the magnetization of the reference layer. When a spin-polarized current flows from the fixed layer to the free layer with antiparallel magnetization then they are aligned in parallel. When a spin-polarized current flows from the free layer to the fixed layer with parallel magnetization, then the magnetization of the free layer is reversed to an antiparallel direction, which is ascribed to the action of the electrons reflected from the field layer [9.57].

Calculations of MRAM elements with perpendicular magnetization (see Fig. 9.17a) based on spin torque switching with dynamic micromagnetic modeling

Table 9.2 Projected performance of MRAM, SMT MRAM, and conventional semiconducting memories [9.50]

	Standard			SMT			SMT
	MRAM (90 nm)[a]	DRAM (90 nm)[b]	SRAM (90 nm)[b]	MRAM (90 nm)[a]	Flash (90 nm)[b]	Flash (32 nm)[b]	MRAM (32 nm)[a]
Cell size (μm^2)	0.25	0.25	1–1.3	0.12	0.1	0.02	0.01
Mbit/cm^2	256	256	64	512	512	2500	5000
Read time (ns)	10	10	1.1	10	10–50	10–50	1
Program time (ns)	5–20	10	1.1	10	$0.1–10^8$	$0.1–10^8$	1
Program energy/bit (pJ)	120	5	5	0.4	$3–12\times10^4$	1×10^4	0.02
Endurance	Needs refresh $>10^{15}$	$>10^{15}$	$>10^{15}$	$>10^{15}$	$>10^{15}$ read $>10^6$ write	$>10^{15}$ read $>10^6$ write	$>10^{15}$
Nonvolatility	Yes	No	No	Yes	Yes	Yes	Yes

MRAM = magnetic random-access memory. SMT = spin momentum transfer; DRAM = dynamic random-access memory; SRAM = static random access memory

[a]MRAM values according to [9.50]

[b]These values are from the International Technology Roadmap for semiconductors [9.50]

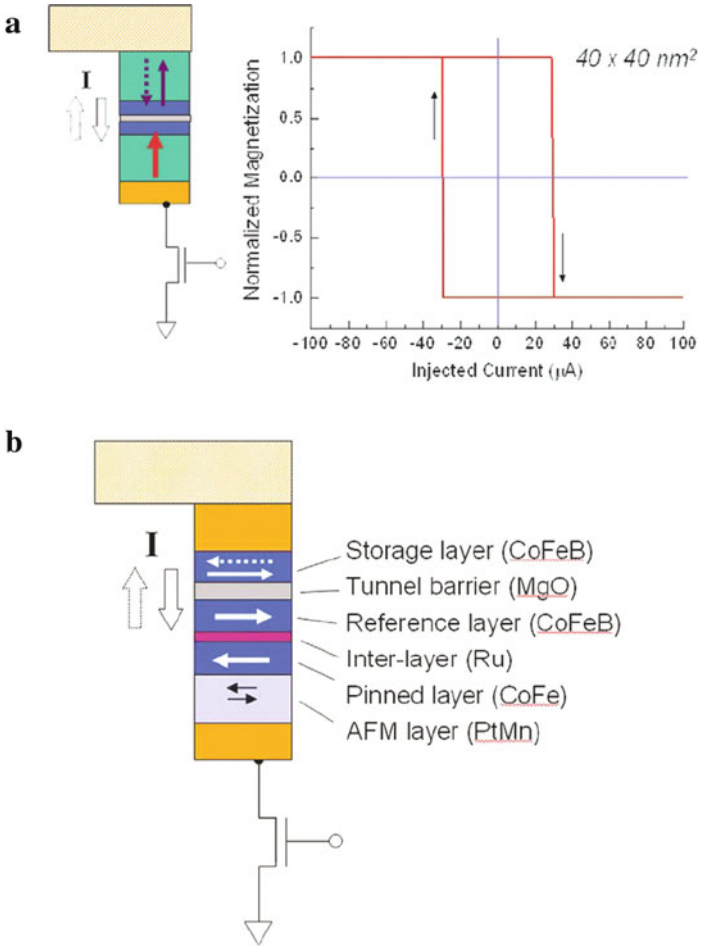

Fig. 9.17 (**a**) Calculated magnetic switching of the free-storage layer of a perpendicular magnetic tunneling junction (MTJ) memory element by direct current injection using spin torque. The magnetization in the MTJ element is perpendicular and the junction area is 40 nm × 40 nm. The perpendicular magnetization can be accomplished by using materials with magnetocrystalline anisotropy that forces the magnetization to be oriented along certain crystallographic axes. The magnetization of the two nanosized layers (*green* and *blue*) within a bilayer is strongly coupled by the ferromagnetic exchange energy, so that the magnetization of the thinner layer is completely perpendicular to the film. The anisotropy strengths of the two bilayers are chosen to be different, yielding different switching field thresholds which enable well-defined parallel and antiparallel states to be reached. The two spin-polarization layers adjacent to the tunnel barrier are assumed to be $Co_{90}Fe_{10}$. A switching current threshold of 30 μA is obtained. (**b**) Schematic of Sony's spin-RAM memory element with direct current injection using spin torque to switch the free-storage layer. (Reprinted with permission from [9.57]. © 2006 Elsevier)

have suggested that such a design may enable MRAM chips to reach many gigabits of storage capacity with low operating power [9.57].

Freescale Semiconductor Comp. has shipped 4 Mbit toggle MRAM devices in 2006 where writing is performed via magnetization reversal of the free-storage layer in an MTJ induced by the magnetic fields generated by the current pulses in the writing lines. The 4 Mbit chip has a relatively small bit count, but applications where battery backup (which cost money and space) can be eliminated will benefit by replacing SRAM or flash with MRAM. This represents the commercial emergence of a truly new memory technology [9.58].

The first on-chip demonstration of a spin-torque-operated non-volatile memory device, a 4 kbit MRAM device named spin-RAM, has been performed by Sony Company in 2005. In this demonstration, the memory elements (see Fig. 9.17b) are CoFeB/MgO/CoFeB MTJs with a tunneling magnetoresistance (TMR) ratio of >160% and a low RA (resistance-area) product of 20 $\Omega\ \mu m^2$ [9.57].

9.4.3 Ferroelectric Random-Access Memories (FeRAM)

Ferroelectric random-access memory (FeRAM) is a type of non-volatile RAM that uses a ferroelectric film as a capacitor for storing data. FeRAM has low access times, high-speed read/write operations, comparable to volatile dynamic RAM (DRAM), it offers the advantages of easy embedding into large-scale integration (LSI) circuits, and it exhibits low power consumption [9.59].

A conventional memory cell for storing one data bit is composed of a cell-selection transistor and a capacitor in the case of a 1T1C (one transistor, one capacitor)-type FeRAM. For higher reliability, the number of transistors (T) and capacitors (C) has been enhanced. In commercially available FeRAMs, PZT [$Pb(Zr_{0.3}Ti_{0.7})O_3$] or SBT ($SrBi_2Ta_2O_9$) is used as ferroelectric material. In order to realize a high-speed system, LSI circuits with embedded non-volatile RAM, a 6T4C type FeRAM (see Fig. 9.18) with a non-destructive readout, unlimited endurance to read/write cycling, an access time of < 10 ns, and a compatibility with standard CMOS LSI components have been developed (see [9.59]). The memory cells in 6T4C-type FeRAMs are larger than those in SRAMs but can be scaled down more easily than in conventional FeRAMs.

Another type of ferroelectric memory, called FET-type FeRAM, is developed from an MFSFET (metal-ferroelectric-semiconductor FET) transistor, in which the gate insulator is composed of a ferroelectric material. In this FET, the polarization direction of the film can be read out non-destructively using the drain current. Based on $Ba_4Ti_3O_{12}$ films, FeRAMs have been developed to be embedded into a complementary metal oxide semiconductor (CMOS) device. This FeRAM with a size of 180 nm exhibits extended read cycle endurance with more than 10^{11} cycles [9.60].

Fe-RAM embedded LSI circuits have been used in smart cards, radiofrequency identification (RFID) tags, and as a replacement for battery-backed-up static RAMs

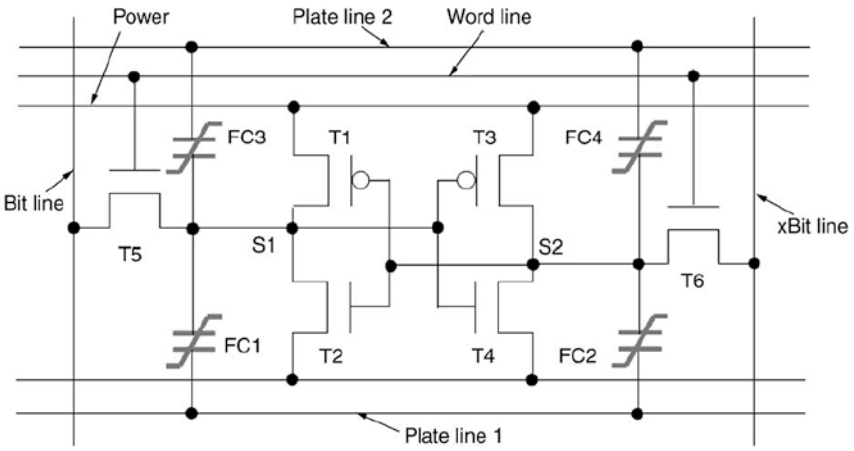

Fig. 9.18 Memory cell circuit of a 6T4C (six transistors, four capacitors) –type FeRAM; FC = ferroelectric capacitor. (Reprinted with permission from [9.59]. © 2004 Materials Research Society)

(BBSRAM), as well as in many other systems on a chip (SoC) (see [9.59]). Recent studies showed that material volumes down to $(20\ \text{nm})^3$ can be ferroelectric and, by making use of scanning probe techniques, storage densities up to 1.5 Tbit/in^2 could be demonstrated [9.61]. Ferroelectric polymers [9.62, 9.63] can be easily transformed into high-density arrays of nanostructures by a nanoembossing protocol, with integration densities larger than 33 Gbits/inch^2 [9.63]. Each nanocell shows a narrow square-shaped hysteresis curve, with low energy losses and a coercive field of $\sim 10\ \text{MVm}^{-1}$, well below previously reported bulk values.

9.4.4 Resistance Random Access Memories (ReRAMs)

Resistance random access memories (ReRAMs) are capacitor-like structures composed of insulating or semiconducting metal oxides, manganites, or titanates that exhibit reversible resistive switching on applying voltage pulses. Recent studies indicate that a thermal or electrochemical redox reaction in the vicinity of the interface between the oxide and the metal electrode is a plausible mechanism for resistive switching (see [9.64, 9.65]).

In the resistive switching phenomenon, a large change of resistance (>1,000%) occurs on applying pulsed voltages (Fig. 9.19). The resistance of the cell can be set to a desired value by making use of an appropriate voltage pulse, with a switching velocity faster than a few nanoseconds [9.66]. Prototype ReRAM devices composed of $Pr_{0.7}Ca_{0.3}MnO_3$ (PCMO) and NiO have been demonstrated recently by Sharp Corporation [9.67] and Samsung [9.68], respectively. However, an integrated circuit

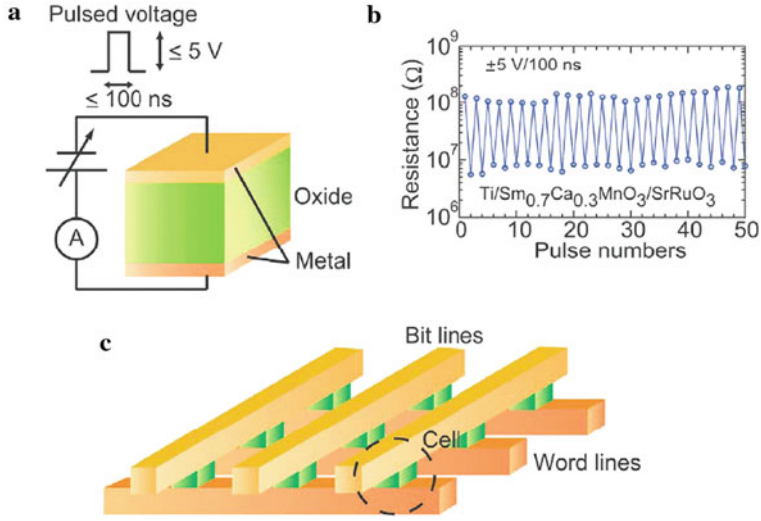

Fig. 9.19 (**a**) Diagram of a ReRAM memory cell with a capacitor-like structure in which an insulating or semiconducting oxide is sandwiched between two metal electrodes. (**b**) Resistive switching in a $Ti/Sm_{0.7}Ca_{0.3}MnO_3/SrRuO_3$ (MIM) cell at room temperature. By applying a pulsed voltage of ±5 V, the resistance of the cell changes reversibly between high- and low-resistance states. (**c**) Diagram of a cross-point memory structure. Word and bit lines are used for selecting a memory cell and writing/reading data respectively. (Reprinted with permission from [9.64]. © 2008 Elsevier)

ReRAM memory, consisting of a sufficient number of cells to be practical, has not yet been demonstrated [9.64].

Based on the *I*–*V* characteristics, two different switching behaviors – unipolar and bipolar – can be observed in different materials [9.64]. The unipolar switching process in, e.g., NiO is ascribed to the formation of filamentary conduction paths (Fig. 9.20) occurring presumably in the grain boundaries [9.69]. In contrast, in bipolar-type switching as, e.g., in a $Ti/La_2\ CuO_4/La_{1.65}Sr_{0.35}CuO_4$ cell [9.64], electronical migration of oxygen ions (by a vacancy mechanism) in the vicinity of the interfaces is regarded as the driving force [9.70–9.72].

9.4.5 Carbon-Nanotube (CNT)-Based Data Storage Devices (NRAM)

Carbon-nanotube (CNT)-based data storage devices (NRAM) show fast write and read speeds, high cell densities, and allow for non-volatile operation [9.37]. Designs of CNT-based electromechanical data storage devices may exploit CNTs as both molecular device elements and molecular wires for the read–write scheme.

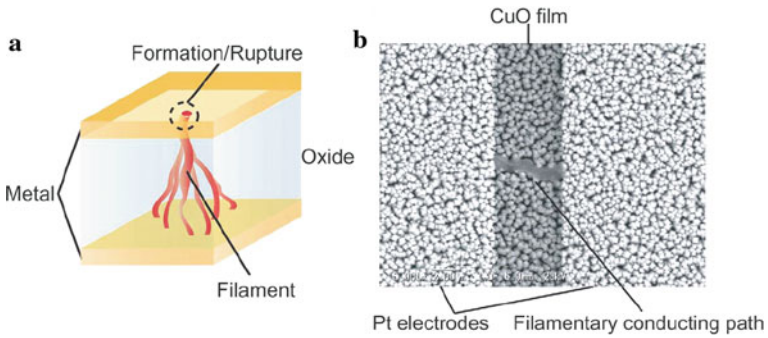

Fig. 9.20 (**a**) Proposed model for unipolar switching of a Pt/NiO/Pt (ReRAM) cell with filamentary conduction paths. (**b**) Scanning electron micrograph of a filamentary conduction path in a CuO film between Pt electrodes with a distance of 5 μm. (Reprinted with permission from [9.64]. © 2008 Elsevier)

The achievement of the controlled and reversible telescopic extension of multiwalled CNTs [9.73] led to a suggestion of an electromechanical switch, operated through the electrostatically initiated sliding of the inner core of a multiwalled CNT out of its sleeve (Fig. 9.21). The device requires a < 10 V of pull-in voltage on the drain electrode and <100 V of pull-out voltage on the gate electrode to produce reversible "0 → 1" conductance cycles with extremely fast switching (see Table 9.3).

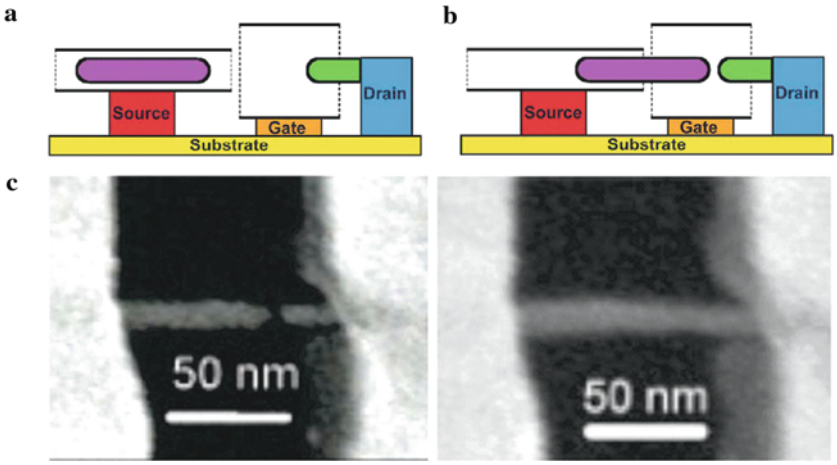

Fig. 9.21 A three-terminal memory cell based on telescoping carbon nanotubes. An all-carbon memory cell with a CNT attached to the gate electrode: (**a**) in non-conducting state "0" and (**b**) in the conducting state "1". (**c**) Scanning electron micrographs of a memory cell with a flat gate electrode [9.37, 9.74]. (Reprinted with permission from [9.37]. © 2008 Elsevier)

Table 9.3 Operational parameters of electromechanical data storage devices based on telescoping carbon nanotubes; for example see [9.37]

Type of study	Linear size, nm	Pull-in voltage, V	Operation frequency, GHz
Experiment	300	4–10	>1
Theory	5–60	6	<100

Memory devices based on CNTs (NRAM) may allow, at least in theory, storage densities higher than those of DRAM (see Table 9.3). Nantero Inc. has recently demonstrated a prototype of a 22 nm NRAM switch and suggested an NRAM scale down below the 5 nm technology node [9.37]. All these advances, however, will become commercial reality only if radical changes in processing are found that gain precise control over the number and spatial location of CNTs over large areas [9.37].

9.4.6 Magnetic Domain Wall Racetrack Memories (RM)

The roadmap for memories means that the size of the memory cell will need to go below 30 nm until 2013. This is made possible by developments that allow multiple bits of information to be stored in magnetic domain walls. This leads to the development of the racetrack memory [9.75]. The controlled movement of domain walls (DWs) in magnetic nanowires by short pulses of spin polarized current (see Sect. 8.7) gives promise of a non-volatile memory device, the magnetic racetrack memory (RM) [9.76–9.79], with the high performance and reliability of conventional solid-state memory but at low cost of conventional magnetic disc drive storage. The racetrack memory is, furthermore, an example of the move toward 3D microelectronic devices.

A domain wall in the section A and B of a nanowire (Fig. 9.22a) can be created by a current pulse from a pulse generator (PG-1 or PG-2) into line A. A current of a density of $\sim 2\times10^8$ A/cm^2 that flows into the nanowire drives the DW along the nanowire between A and B. The position of the DW can be controlled by varying the injection pulse length without using any magnetic field. Sequential injection and removal of two domain walls is detected by specific changes in the nanowire resistance (Fig. 9.22b, c). A DW shift register memory, namely a three-bit unidirectional serial-in, serial-out memory, in which the data are coded as the magnetization direction of individual domains, is shown in Fig. 9.23a. A left-pointing domain represents a 0 and a right-pointing domain a 1. The data was written into the left-most domain, was shifted by two domains, and then read from the state of the right-most domain. For example, when the data sequence 010 111 is written into the register, the resistance and the corresponding magnetization configuration

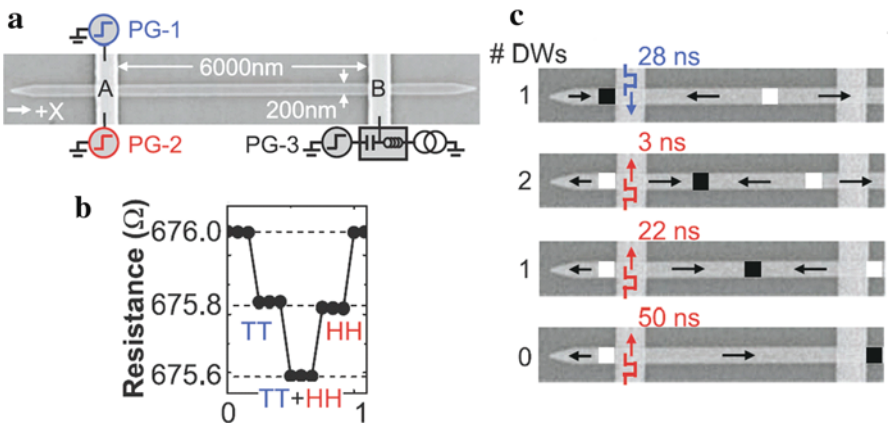

Fig. 9.22 (**a**) Scanning electron micrograph of a permalloy nanowire and the electrical contact lines A and B. PG, pulse generator. (**b**) Variation of the nanowire dc resistance and (**c**) illustration of the corresponding motion of tail-to-tail (TT; *white squares*) and head-to-head (HH; *black squares*) domain walls. *Black arrows* represent the magnetization direction within each domain, *blue* and *red arrows* represent the electron flow directions. (Reprinted with permission from [9.77]. © 2008 AAAS)

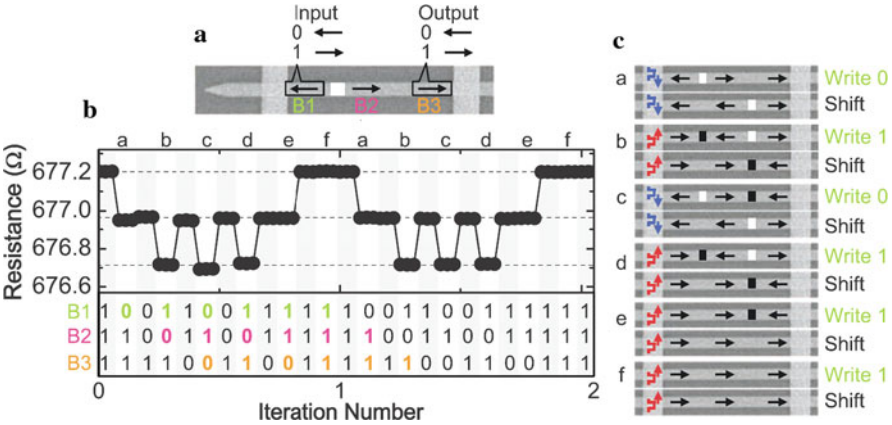

Fig. 9.23 Three-bit magnetic domain wall (DW) shift register. (**a**) The data is encoded by the magnetization direction of three domains in the nanowire. (**b**) Variation of the nanowire resistance when a pulse sequence is used to write and shift along the register the sequence 010 111 two times in succession. The *light* and *dark* regions indicate writing and shifting operations, respectively. The table shows the corresponding evolution of the states of the three bits during these operations. The *highlighted* digits show how the input bit sequence is transferred to the output after two write/shift operations. (**c**) Schematic illustration of the shift-register operation. *White squares* and *black squares* represent tail-to-tail and head-to-head DWs, respectively. *Black arrows* indicate the magnetization direction of each domain. *Blue* and *red arrows* show the electron flow directions. (Reprinted with permission from [9.77]. © 2008 AAAS)

evolved as shown in Fig. 9.23b, c. In Fig. 9.23b, the light regions correspond to write operation and the shaded regions to a shift operation. The input sequence is accurately transferred to the output after two write/shift operations, with a cycle time to write and shift one bit of ∼30 ns. The rapid motion of a series of DWs using nanosecond current pulses not only demonstrates the viability of a shift register memory but also indicates the possibility of current-controlled DW-based logic devices [9.77].

The concept of racetrack memories is to crate U-shaped wire loops, ∼100 nm in diameter, containing regions magnetized in opposite directions over a total length of tens of microns (Fig. 9.24). This series of domain walls, which represents a series of bits, could be passed up and down the nanowire (Fig. 9.24f) past reading or writing devices. The process involves the motion of only magnetic moments – no atoms move, and, therefore, exhibits no wear or fatigue. Each column may have its own reading/writing device with a read/write velocity of 100 m/s at a bit size of ∼1 μm. This makes the system much faster than disk drives with only one reading/writing device, yielding an average access time for RM of 10–50 ns, as compared to 5 ms for a hard disc drive (HDD) and perhaps ∼10 ns for advanced MRAM [9.79]. The RM data storage may be cheaper even than flash [9.78] because one could store in the same area of Si, that stores one bit in flash, 10 bits in the RM technology. If RM could replace disk drives and flash, it opens up the possibility of simplifying computers by reducing the number of memory storage technologies on which they rely. A challenge for the development of racetrack memories is the high-current densities of $\sim 2 \times 10^8$ A/cm^2 required at present for domain wall motion. The critical current can, however, be substantially reduced by resonantly amplifying the DW's oscillatory motion at pinning centers making use of properly engineered current pulse sequences (see [9.79]).

9.4.7 Single-Molecule Magnets

Single-molecule magnets (SMMs; see Sect. 8.8) could be a promising alternative for high-density data storage, but they need to be connected to a conducting surface. SMMs based around four atoms of iron with oxygen, carbon, and sulfur atoms can be attached to a gold substrate by self-assembly, showing the signature hysteresis loop at 0.5 K and a magnetization maintained for about 220 s [9.80].

9.4.8 10 Terabit/Inch^2 Block Copolymer (BCP) Storage Media

Ordered arrays of cylindrical nanodomains of block copolymers (two chemically dissimilar polymers joined together) 3 nm in diameter (Fig. 9.25) with areal densities in excess of 10 terabits per square inch can be produced [9.81]. These BCP films are promising candidates for the generation of ultrahigh density storage media that have the potential of being addressable [9.81].

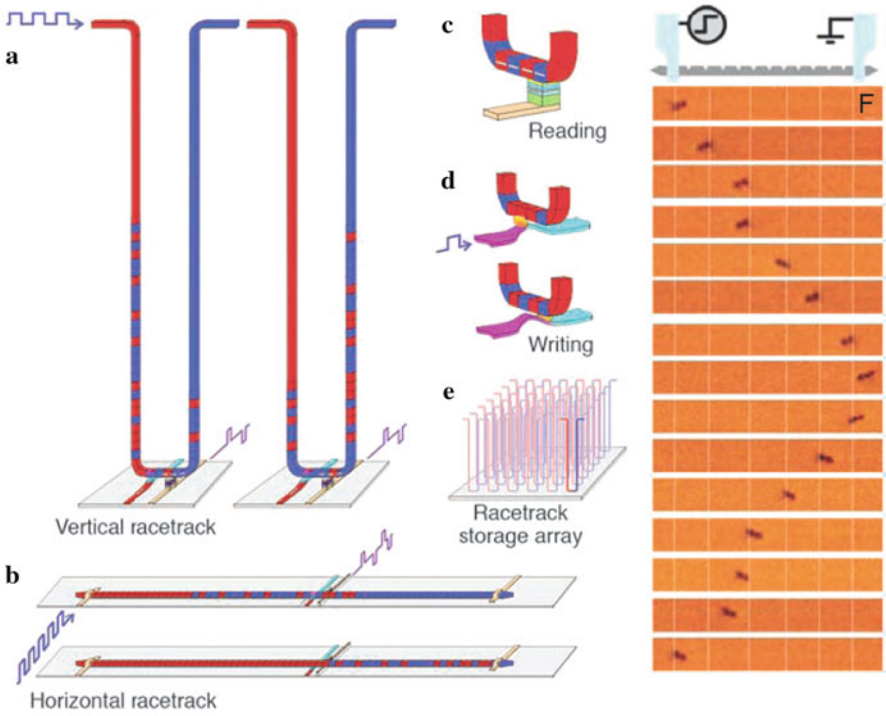

Fig. 9.24 The racetrack memory is a ferromagnetic nanowire, with data encoded as a pattern of magnetic domains. Pulses of highly spin-polarized current move the pattern of domain walls (DWs) coherently along the length of the wire past read and write elements. (**a**) A vertical-configuration racetrack offers the highest storage density in a U-shaped nanowire normal to the plane of the substrate. The two cartoons show the magnetic patterns before and after the DWs have moved down one branch of the U, past the read and write elements, and then up the other branch. (**b**) A horizontal configuration uses a nanowire parallel to the plane of the substrate. (**c**) Reading data from the stored pattern is done by measuring the tunnel magnetoresistance of a magnetic tunnel junction element connected to the racetrack. (**d**) Writing data is accomplished, for example, by the fringe fields of a DW moved in a second ferromagnetic nanowire oriented at right angles to the storage nanowire. (**e**) Arrays of racetracks are built on a chip to enable high-density storage. (**f**) Magnetic force microscopy (MFM) for imaging the motion of a single tail-to-tail vortex DW. The cartoon at top shows a schematic of the experiment. A nanowire with a series of notches for pinning the domain walls was connected to electrical contacts to allow for injection of current pulses. Experimental results are shown for a 40 nm thick, 100 nm wide permalloy nanowire with 11 triangular notches located 1 μm apart; a part of the nanowire with six notches, indicated by vertical *white lines*, is shown. Single current pulses, 8 V (26 mA) and 14 ns long, were applied between each image sequentially from top to bottom, applying pulses with negative polarity for the first eight images and pulses with positive polarity for the last seven images. (Reprinted with permission from [9.79]. © 2008 AAAS)

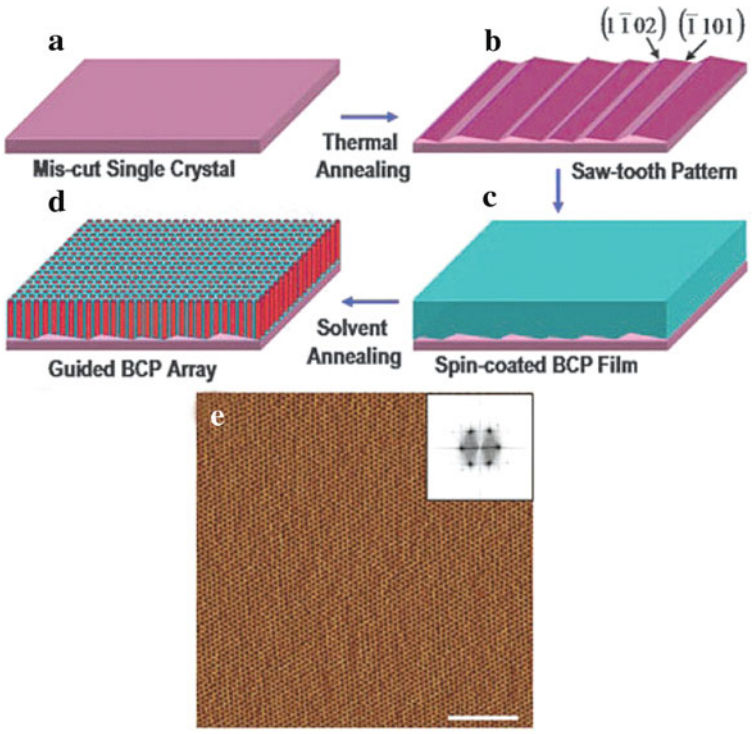

Fig. 9.25 (**a**–**d**) Schematic illustration of the strategy used for generating block co-polymer (BCP) cylindrical nanodomains on highly oriented facets on a single-crystal sapphire surface (**a**) after annealing at 1500°C to form sawtooth patterns (**b**). (**c**) Smooth polystyrene-*block*-poly(ethylene oxide) (PS-*b*-PEOs) thin films were spin-coated unto these surfaces that, upon annealing in *o*-xylene vapors (**d**), produced highly ordered cylindrical nanodomains oriented normal to the film surface. (**e**) Atomic force microscopy (AFM) of highly ordered PS-*b*-PEO nanodomains in PCB thin films. Scale bar, 100 nm. (Reprinted with permission from [9.81]. © 2009 AAAS)

9.5 Magnetic Hard Disks and Write/Read Heads

More than half a century of progress in magnetic data storage has fundamentally changed information technology (see [9.82–9.84]). Starting with the IBM350 disk drive in 1956 with over fifty 24 in disks and a total of 4.4 Mbytes storage capacity (0.002 Mbits/in.^{2}), devices with several hundreds of Gbits/in.^{2} are available at present (see Fig. 9.26) due to rapid down scaling enabled by technical breakthroughs and novel components. Apart from the fast scaling of the bit sizes in the magnetic media, the thickness t of the media of initially 30 μm and initial fly height of the writing/reading heads of ∼20 μm have been decrease up to now into the nanoregime of ∼15 and ∼10 nm, respectively [9.83]. The development from longitudinal to perpendicular recording and future approaches, as well as the structure of write heads

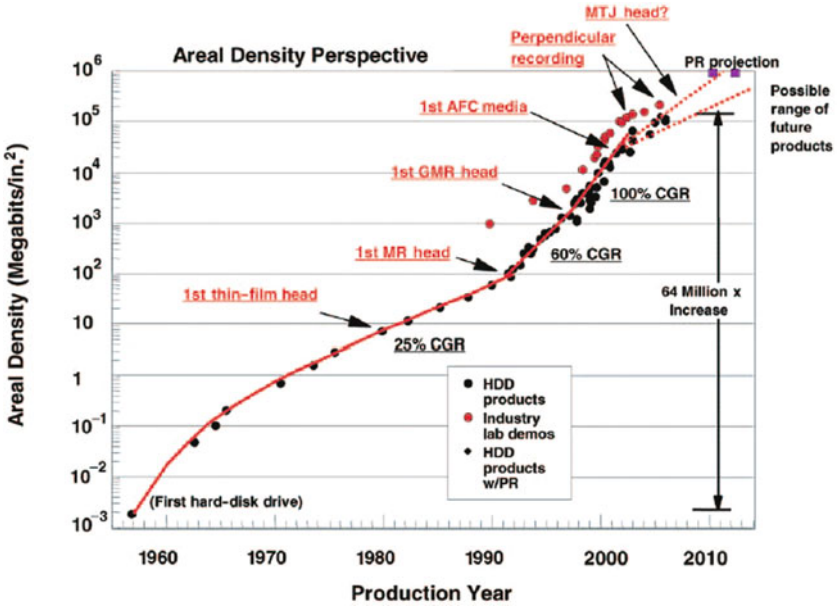

Fig. 9.26 Storage density of magnetic hard disk drives as a function of calendar year. The compounded growth rate (CGR) for some periods are indicated, as well as the technical breakthroughs. MR stands for the introduction of the magnetoresistance head, GMR for the giant magnetoresistance, AFC for antiferromagnetically coupled media, and PR for the introduction of perpendicular recording into the manufacturing of hard disk drives (HDDs). (Reprinted with permission from [9.82]. © 2006 Materials Research Society)

and particularly of giant magnetoresistance read back heads, will be outlined here. The areal density of magnetic recording on flexible tape is at present [9.85] two to three orders of magnitude lower than on hard disc drives. The mechanical and magnetic properties of materials that play a key role in the future of tape have been discussed recently [9.85].

In the magnetic recording process, the bits (containing each about 100 grains) are written as magnetization patterns, with the magnetization pointing either "left" or "right" within the plane of the magnetic medium for longitudinal recording and "up" or "down" for perpendicular recording. Typically, hcp Co alloys with uniaxial anisotropy are used for the recording media, i.e., with the easy magnetic axis along the c-axis. The energy that keeps the magnetization on the easy axis is $K_U V$, where K_U is the magnetocrystalline anisotropy energy density and V the volume of the grain. The scaling down of media is limited by thermal instability of the magnetization direction (bit) when $K_U V$ becomes comparable to the thermal energy $k_B T$, i.e., the transition probability or relaxation rate is given by $r = f_0 \exp(-K_U V/k_B T)$ with $f_0 = 10^{10} \ldots 10^{11}$ Hz. The minimum energy needed to maintain stability for > 10 years is $K_U V > 55\, k_B T$. Reduction in V for higher storage density can be countered by increasing K_U. Doping of Co with Pt is highly effective in increasing K_U, as the large atomic radius (0.1387 nm) engenders an expansion of the Co c-axis relative

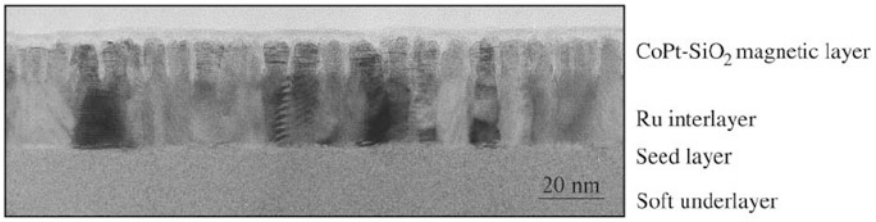

Fig. 9.27 Cross-sectional transmission electron micrograph of a typical perpendicular recording medium design. (Reprinted with permission from [9.84]. © 2006 Materials Research Society)

to the *a*-axis. However, K_U increases are limited by available write fields needed to overcome the media's coercive field, $\sim K_U/M_S$, where M_S is the saturation magnetization. The combination of signal-to-noise ratio (SNR) requirements, write-field limitations, and thermal activation of small particles is commonly referred to as the superparamagnetic limit. Since it is the grain volume V and not the grain area that enters in the magnetic energy $K_U V$, it is attractive to increase the film thickness – that is to make media with "tall and slim" grains. Film thicknesses up to 15–20 nm are indeed common for perpendicular recording media. The grain size in perpendicularly oriented (0001) Co alloys is dominated by the template grain size of the Ru alloy sublayer with a high surface energy, leading to a finely dispersed nucleation density, and a similar hcp structure and lattice parameter to enable parallel alignment with the top Co alloy (Fig. 9.27). The seed layer establishes the crystallographic texture for the Ru interlayer grown above. For the seed layer, low-surface-energy fcc materials are employed that wet the amorphous soft underlayer (SUL). The fcc (111) planes make suitable templates for hcp (0001) growth when the lattice parameters match. The porosity between the magnetic particles and the SiO_2 insulating layer are introduced in order to suppress quantum mechanical magnetic exchange coupling between the grains which causes a magnetic clustering of the grains and therefore a transition jitter [9.84].

9.5.1 Extensions to Hard Disk Magnetic Recording

A very promising extension to perpendicular recording is *composite media* [9.86] of a two-layer structure with materials of different properties. Material 1 has such a high anisotropy field $H_A = 2K_U/(\mu_0 M_S)$ that it cannot be written with available head fields, and Material 2 serves as a switching assist. Making use of a properly tuned exchange coupling between the two layers, the result is most effective when the contrast between the materials is well pronounced: $M_{S2}/M_{S1} \gg 1$ and $H_{A2}/H_{A1} \ll 1$. Another approach makes use of the effect that for all magnetic materials the anisotropy decreases when increasing the temperature. The basic idea of *heat-assisted magnetic recording* is to heat the media during the writing process

to temporarily lower the switching field [9.87]. The full anisotropy remains available during storage. Demonstrations of *perpendicular recording* [9.88, 9.89] have reached $\sim$ 400 Gb/in^2, with the potential for values of 1 Tbit/in^2. The superparamagnetic limit is also addressed by *bit-patterned media*: rather than recording one bit on a large number (50–100) of grains as nowadays, one single grain or magnetic island represents one bit. The entire volume of the bit contributes to the magnetic energy, and stable media can be achieved with much lower anisotropies [9.90] and with prospects of storage densities up to 5 Tb/in^2 [9.91] but, simultaneously, a completely new set of challenges for manufacturing [9.92] emerges. Still higher data storage densities are promised by *current-induced switching* of the magnetization as tentatively studied by spin-polarized scanning tunneling microscopy of 7 nm^2 Fe islands ($\sim$ 100 atoms) on a substrate [9.93] (see Sect. 8.1.2).

9.5.2 Magnetic Write Head and Read Back Head

For perpendicular magnetic recording, the writing is accomplished by a miniature electromagnet: a time-varying current in a conductor wrapped around the main pole (Fig. 9.28) generates the write flux that is sent through the magnetic storage layer, then through a magnetically soft underlayer (SUL) beneath the storage layer, and finally reenters the head structure through the return pole. The storage media can be thought of as traveling through the deep gap field of the head rather than the fringefield, thus, higher-coercivity media can be written.

The reading back of the data on the magnetic media occurs by measuring the stray fields (as described below) originating from transitions between opposite magnetization and not the magnetization itself. As the read density increased, the signal from the recorded transitions decreased and more sensitive detectors such as the giant magnetoresistance (GMR) head or spin-valve (since 1997), which enabled a thousand-fold increase in the storage capacity of hard disc drives in the last decade [9.79], were required with a GMR effect of 15% today. A view of this device, looking up from the media, is shown in Fig. 9.29. The GMR sensor is sandwiched between micrometer-thick magnetic shield layers (with a shield-to-shield spacing of 50 nm) which provide down-track spatial magnetic resolution by absorbing the magnetic flux from nearby media transitions. The sensor itself is lithographically patterned to half the track width, W, which is about 100 nm. As the track width scales to smaller dimensions, this is pushing magnetic recording past semiconductor processing in terms of the smallest feature size.

The basis of the GMR effect (see Sect. 1.4) is contained in only three layers: a cobalt alloy magnetic reference layer, a non-magnetic Cu spacer layer, and second magnetic free layer of a Co alloy. A current flowing in the magnetic layers is spin-polarized and the probability of electron scattering as they move between the magnetic layers depends on the relative orientation of the magnetization of these layers. This is a minimum, R_0, when the magnetizations of the free layer and reference layer are parallel. Spin-dependent scattering increases the resistance by maximum ΔR as the layer magnetizations deviate from parallel (see Sect. 1.4).

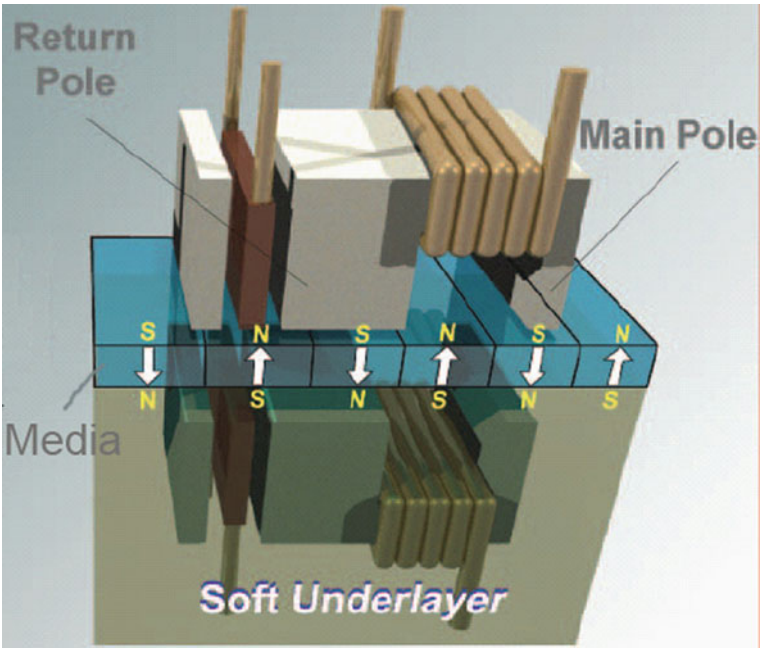

Fig. 9.28 Schematic illustration of perpendicular recording. The writing is performed by the main pole (on the *right*). The magnetic write flux penetrates the media and is conducted via the magnetically soft underlayer (SUL) back into the return pole. The field configuration in the presence of the SUL can be viewed as if the head structure were imaged in the SUL. (Reprinted with permission from [9.84]. © 2006 Materials Research Society)

In a GMR read head the magnetic moment of the reference layer points perpendicular to the medium surface. With zero field from the medium, the free layer moment points perpendicular to this direction ($\theta = 90°$). When the head passes over a magnetic transition in the medium, the free layer makes only a $\sim 10°$ deviation from 90°. The output signal is, then, fairly well linear with the field and the head uses only a 3% fraction of the $\Delta R = 15\%$ GMR effect.

The detailed structuring of the tiny and most sensitive GMR detector (Fig. 9.29), which impressively demonstrates the electronic, magnetic, and chemical interplay and adjustment of the various materials on the nanoscale, is discussed in the following. A typical underlayer structure is Ta (3 nm)/ NiFeCr (3 nm)/Ni Fe (0.8 nm). The Ta provides good adhesion and promotes a (111) texture, which is beneficial for the magnetic properties of the free layer. The deposition of NiFe gives rise to crystallization of NiFeCr to grain sizes as much as 22 nm, which decreases grain boundary scattering and increases the output of current-generation spin valves by 30% [9.83]. The next layer is the antiferromagnetic IrMn (for the properties of antiferromagnetic materials see [9.83]), which "pins" the ferromagnetic layer's magnetic moment through a mechanism called exchange anisotropy. This prevents the moment of the

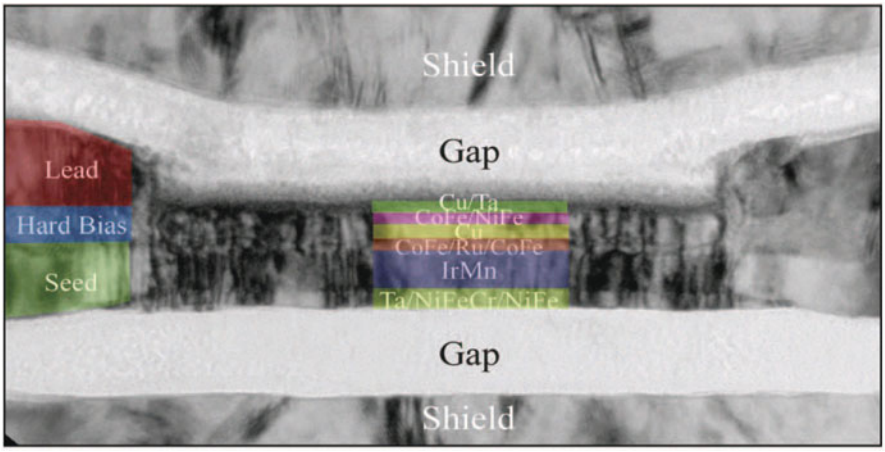

Fig. 9.29 Transmission electron micrograph of a giant magnetoresistance spin valve read head viewed as looking up at the head from the media. The 120 nm wide sensor is a multilayer stack. In addition to providing the sense current, the leads contain a magnetically hard bias layer that applies a small magnetic field to the sensor. The magnetic shields ensure that the sensor detects only the field from a single-magnetic transition at a time. (Reprinted with permission from [9.83]. © 2006 Materials Research Society)

ferromagnetic layer from rotating in moderate magnetic fields, making it useful as a reference layer. The magnetic CoFe/Ru/CoFe reference layer and the magnetic CoFe/NiFe free layer are coupled antiferromagnetically through the Cu spacer layer via the long-range Ruderman–Kittel–Kasuya–Yosida (RKKY) interaction. The Cu spacer layer not only separates the magnetic layers, but, since its band structure closely matches that of CoFe, it also allows electrons to pass with little spin-independent scattering, a key feature for GMR transport. In the free layer made of CoFe and NiFe, the $\sim$ 1 nm thick CoFe layer in contact with Cu gives high GMR and responds in contact with NiFe, due to a magnetic softening, more readily to low fields than CoFe alone. In addition CoFe and Cu are immiscible, yielding sharp interfaces, which improves GMR. The spin valve is capped with a Cu/Ta bilayer to protect the device from oxidation during processing.

The spin valve, from the seed layers to the cap, is fabricated in one deposition without breaking vacuum and is patterned afterward. Due to the small sensor dimensions, lithography techniques are used and electron-beam lithography will likely be required in the future. Conductive leads are deposited on the patterned spin valve to provide the sense current. The CoPtCr "hard bias" portion of the leads (see Fig. 9.29) provide a small magnetic bias field to stabilize the free layer, reducing noise. To the complete read head, a top alumina cap and magnetic shield layers are added (see Fig. 9.29). The write head is then fabricated on top of this read head (see [9.83]). A single wafer contains approximately 20,000 heads. The heads are finally mechanically lapped to expose the read sensor in the nanostructured device.

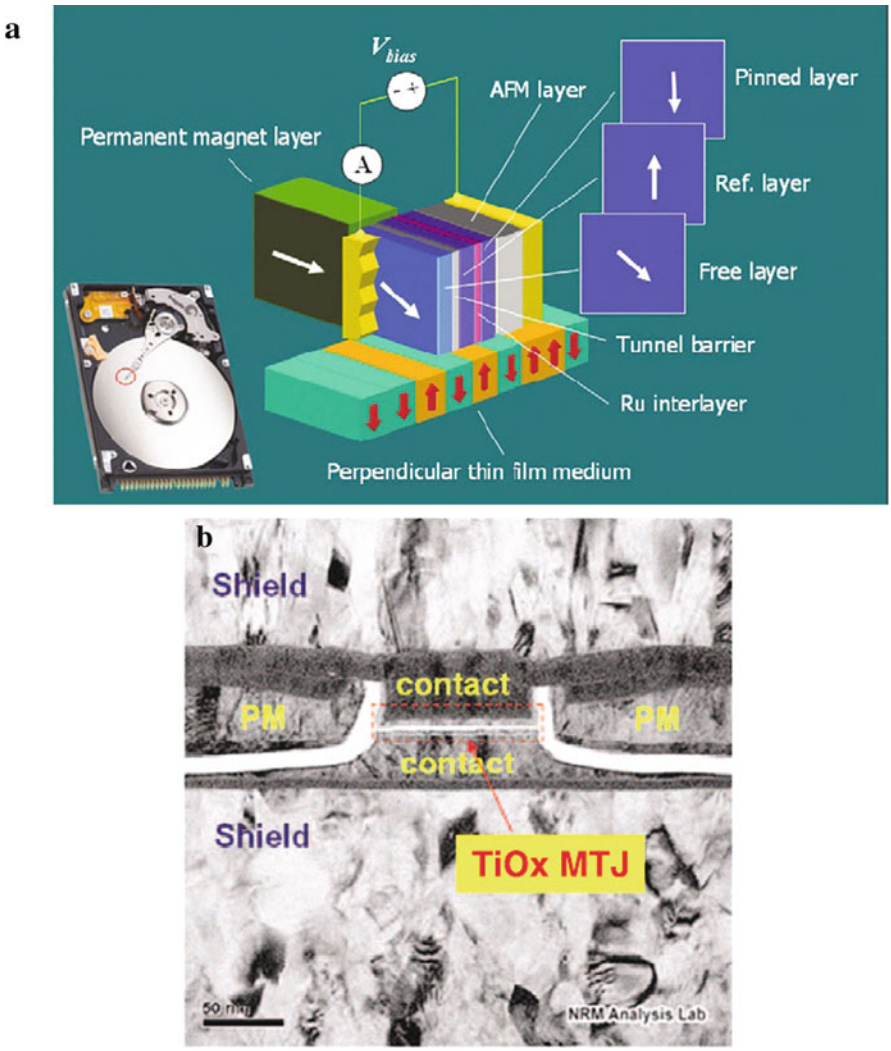

Fig. 9.30 (**a**) Magnetic tunneling junction (MTJ) reads head for a hard disk drive (HDD). One magnetic electrode is a free layer, and its magnetization rotates freely in response to the medium signal field. The magnetic moment of the other electrode is "fixed" through the interlayer magnetic coupling and functions as a reference to the free layer magnetization orientation. (**b**) Transmission electron micrograph of a commercial MTJ read head with a TiO_x barrier layer, viewed from the magnetic data storage medium, produced by Seagate Technology. (Reprinted with permission from [9.57]. © 2006 Elsevier)

In hard disk drive (HDD) read heads, also magnetic tunnel junctions (MTJs) have been commercialized by Seagate Technology since 2004 (see [9.57]) and many disc drive products have read heads with TiO_x-based MTJs (see Fig. 9.30). The TiO_x insulator provides a low resistance-area (RA) product. This is of importance when higher and higher data storage densities are packed on a disk and the size of the MTJ element needs to be reduced accordingly. In this case, the resistance must be prevented from increasing because this would lead to a longer time constant and – at high resistance – a sufficient current density would stress or damage the tunnel junction [9.57]. In the not-so-distant future [9.57], HDD read heads are very likely to use MgO-based MTJs when the high tunneling magnetoresistance ratio can be combined with an RA value for exceeding the present data rates of already 1 Gbit/s [9.57].

When the magnetic bits get smaller and smaller, this requires the significant reduction of the magnetic spacing which is the vertical distance between the read head and the magnetic storage layer (Fig. 9.31). Reducing the fly height of the read head requires ever thinner carbon films for disk and head protection with a present thickness of 4 nm. For 1 Tbit/in.^{2} devices the magnetic spacing will be 6.5 nm which implies ∼1 nm disk and head overcoat. The ideal material for this would be tetrahedral amorphous carbon (ta-C) which is a diamond-like carbon (DLC) with a maximum C–C sp^3 bond content. This ta-C material has an ultralow roughness (rms roughness ∼ 12 nm) that is independent of the film thickness [9.89].

Between 1997 and 2007 about 5 billion GMR read heads were shipped. Since 2005 these read heads were replaced by TMR (tunneling magnetoresistance in MTJ) and since recently by PMR (perpendicular magnetoresistance) [9.94].

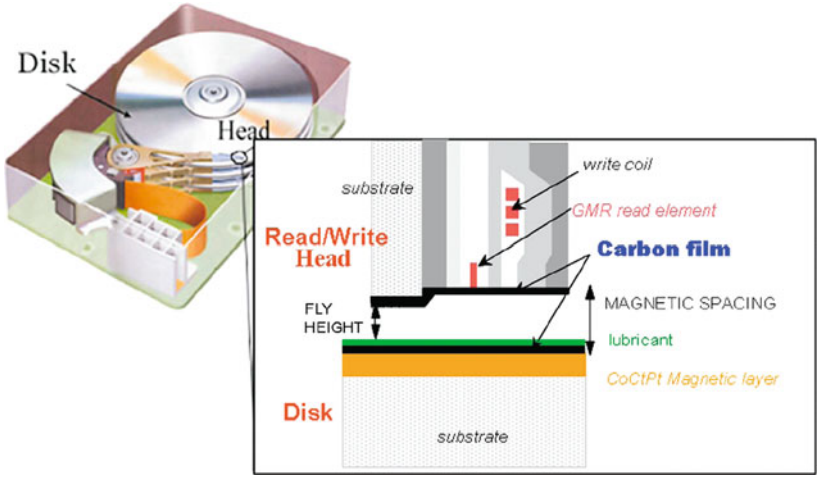

Fig. 9.31 Hard disk architecture. (Reprinted with permission from [9.89]. © 2007 Elsevier)

9.6 Optical Hard Disks

Optical data storage has become ubiquitous as a method for distributing content, archiving data, and managing information [9.95]. The progression of optical storage from high-fidelity stereo compact disks (CDs), storing approximately 74 min of audio, has required the evolution to digital versatile disks (DVDs), to high-definition DVDs and Bluray disks (BDs) (see Fig. 9.32). The disks contain surface structures called pits and lands. A semiconductor laser is used to reflect off of this structure to reconstruct the recorded data (Fig. 9.33). Concurrently with the development of CDs and DVDs, magneto-optical disks were developed which are based on the modulation of light by the magnetic state of the material, with current capacities of many gigabytes and expectations of terabytes of storage capacity (see [9.95]). Multilayer optical recording and holographic data storage may extend the optical storage roadmap to even higher performance. In the following an overview of these optical storage technologies will be given.

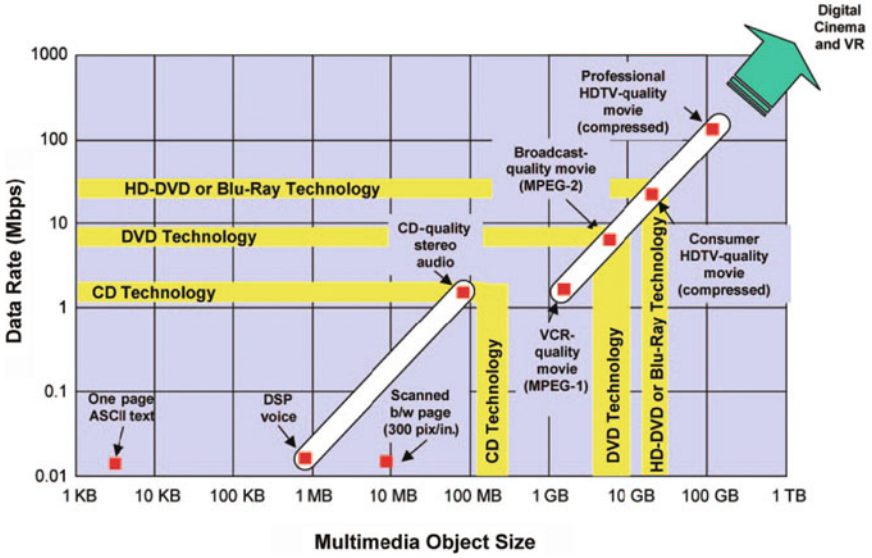

Fig. 9.32 The increase in storage capacity and complexity of multimedia objects has driven improvements in optical storage technologies. CD = compact disk, DSP = digital signal processor, DVD = digital versatile disk, HD-DVD = high-definition DVD, KB = kilobytes, MD = megabytes, GB = gigabytes, TB = terabytes, pix = pixel, Mbps = megabits per second, MPEG-1 = moving pictures expert group standard 1, MPEG-2 = moving pictures expert group standard 2, VR = virtual reality. (Reprinted with permission from [9.95]. © 2006 Materials Research Society)

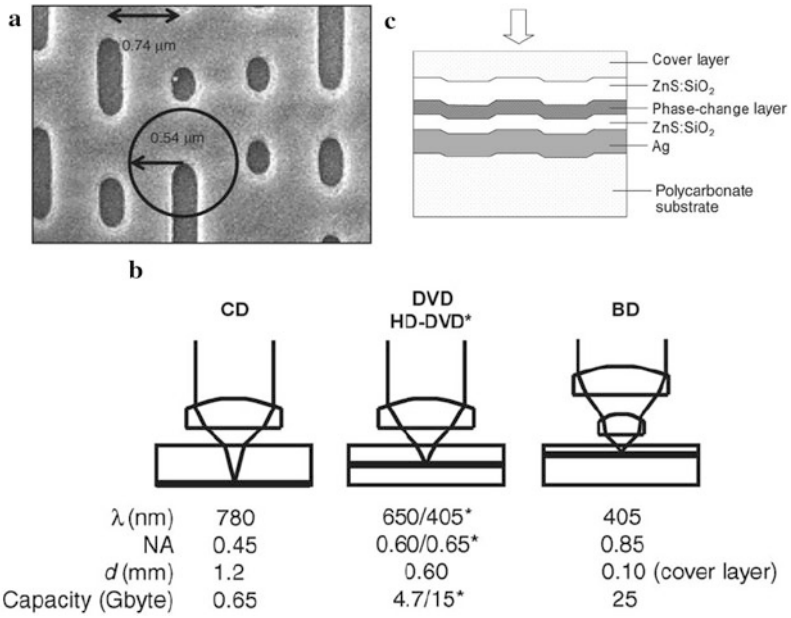

Fig. 9.33 (**a**) Electron micrograph of embossed pits in a DVD-ROM disk (viewed from the *top*). The track pitch is 740 nm, the shortest pit has a length of 400 nm, and the spot radius is 540 nm. (**b**) Roadmap of optical data storage and its key parameters. CD = compact disk, DVD = digital versatile disk, HD-DVD = high-definition digital versatile disk, BD = Blu-ray disk, λ = wave length of the laser light, NA = numerical aperture of the objective lens, and d = thickness of substrate or cover layer [9.96]. (**c**) Schematic illustration of a phase-change stack for blue recording [9.99]. (Reprinted with permission from [9.96] (**a**) (**b**) and [9.99] (**c**). © 2006 Materials Research Society)

9.6.1 Principles and Materials Considerations

A basic component for current optical disk systems is an objective lens with a specific numerical aperture (NA; see Fig. 9.33b) to focus a laser beam with the wavelength λ through a transparent cover layer onto the highly reflective information layer where the diffraction-limited spot radius is given by $s/2 = \lambda/(2\text{NA})$ (see [9.96]). The reflectivity is modulated locally by the optical character (phase or amplitude objects) of the pits/marks. The information is digitally encoded in the lengths of the pits/marks (Fig. 9.33).

In prerecorded read-only memory, the embossed pits act as phase objects. The pit width is smaller than the laser beam to allow for destructive interference between light reflected from the pit and from the neighboring land area. For a high modulation depth of the readout signal, a pit height $H \approx \lambda/4n_0$, with n_0 the index of

refraction of the substrate, is optimum. The accuracy of the pit height replication in the fast molding fabrication process has to be kept within tight limits of a few nanometers.

In recordable or rewritable disks, an additional functional layer is located between the metallic refractive layer (usually Ag) and the transparent cover layer. Also, a spiral pregroove is embossed into the substrate for tracking and addressing purposes in the unrecorded state where the nanometer accuracy is again very important [9.96]. In the case of recordable disks the functional layer is an organic dye layer which decomposes thermally under laser writing and changes locally its complex index of refraction $n + ik$.

In the case of rewriteable disks (CD-RW, DVD-RW, DVD-RAM, BD), which can accommodate writing, reading, erasing, and rewriting of data, the functional layer comprises a thin phase-change layer ($\sim$ 10–15 nm) of, e.g., a chalcogenide alloy such as Ag–In–Sb–Te (see Fig. 9.33c), embedded in dielectric layers. The phase-change layer changes its index of refraction $n + ik$ between the amorphous and the crystalline states [9.40] due to differences in the electronic and chemical structure of the two phases [9.97]. The information is stored by means of amorphous marks which are written by local laser heating and rapid quenching. The change in the amplitude of the reflected light coming from the amorphous mark or the crystalline land is used for reading. Rewriting is effectuated by appropriate heating the amorphous marks for recrystallization and subsequent writing. The data rate, which is one of the key parameters in recording, is limited by the crystallization of the phase-change materials. A high crystallization rate may originate from a high vacancy concentration in the metastable crystalline structure [9.98]. By doping of phase-change Sb_2Te compounds, data rates of 60 Mbit/s for overwriting have been achieved. Another important parameter is the archival life stability. From temperature-dependent crystallization studies of phase-change materials, a lifetime of phase-change recorded data of 1,000 years at a storage temperature of 90°C can be estimated [9.99]. Erasable thermal phase-change recording at storage densities up to 2.2 Tb in^{-2} has been demonstrated (see Fig. 9.34).

It is anticipated that the vast majority of disks in blue recording are write-once disks. In such disks, a cost-effective dye layer could replace the more complex phase-change stack. Dyes sensitive to blue-violet lasers have been tested on prototype BD-R and HD-DVD-R disks (see [9.99, 9.100]). Another option for write-once disks is to replace the phase-change layer (Fig. 9.33c) by a 5 nm Si/6 nm Cu bilayer which by laser illumination transforms irreversibly into a Cu_3Si layer with optical characteristics quite different from those of the components [9.99].

In a CD the numerical aperture NA is typically 0.5 and λ is 780 nm. In a DVD, NA is 0.6 and $\lambda = 650$ nm. A third generation of optical devices with a blue laser of $\lambda = 400$ nm allows a storage density of 20–30 GB per disk [9.95]. In an emerging fourth generation of optical devices with near-field data storage, a dramatic reduction in spot size can be achieved by using a lens with NA >1, known as the solid immersion lens (SIL; Fig. 9.35). It is possible to have a SIL with a refractive index between 1.5 and 3 yielding $\sim$ 100 Gbytes per disk to be reached [9.101]. However, a carefully controlled gap between lens and disk is needed with a transparent coating on the disk in order to protect slider and disk during start-stop and crashes. The

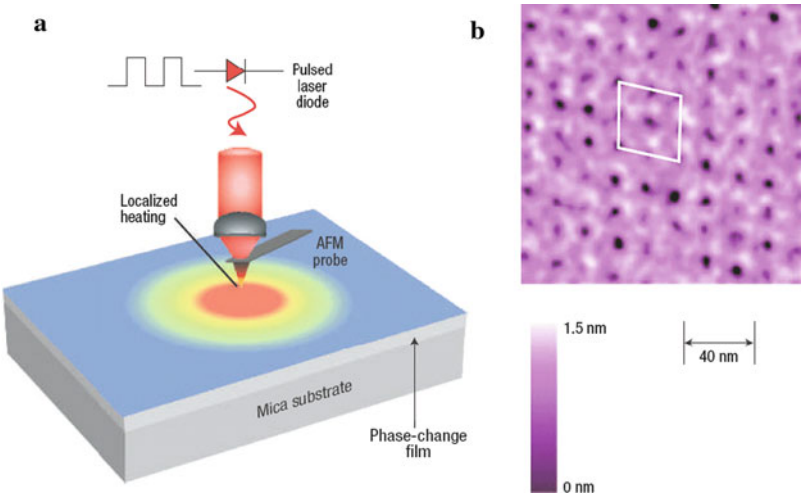

Fig. 9.34 Thermal recording of ultrahigh density phase-change bit patterns. (**a**) Experimental set-up. (**b**) AFM images of an array of crystalline phase-change bits in an amorphous $Ge_2Sb_2Te_5$ matrix with a storage density of 3.3^2 Tb in^{-2}. (Reprinted with permission from [9.47]. © 2006 Nature Publishing Group)

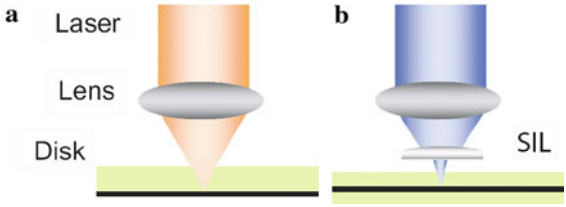

Fig. 9.35 (**a**) Optical data storage technology using far-field optics. (**b**) Near-field data storage technology using a solid immersion lens (SIL). CDs and DVDs use a metallic reflective layer (*black*) sandwiched between a substrate (*green*) and a lacquer surface (not shown). (Reprinted with permission from [9.89]. © 2007 Elsevier)

requirements for this coating can be satisfied by a layer of tetrahedral amorphous carbon with hydrogen (ta-C:H) (see [9.89]).

Approaches to further enhance the information storage density of optical recording exploit simultaneously wavelength, polarization, and spatial dimensions for multiplexing making use of the longitudinal surface plasmon resonance (see Sect. 7.6) of Au nanorods [9.102]. This concept leads to a storage capacity of 1.6 Tbytes for a DVD-sized disk and disk capacities of 7.2 Tbytes with recording speeds up to 1 Gbits/s are envisaged [9.102].

The substrate material has to meet different well-balanced requirements comprising optical, rheological, mechanical, and processing properties. The most appropriate performance profile is reached with BPA-PC and $\sim$ 800,000 tons of polycarbonates were used for ODS production in 2004 [9.96].

9.6.2 Magneto-Optical Recording

Magneto-optical recording (MO) has been first commercialized in 1988 (see [9.103]). Materials and technologies for MO disks may play an important role in recording for ultrahigh densities beyond 1 Tbit/in^2 [9.103].

In this technique the recorded marks are read out by the magneto-optical effect, where the axis of polarization of the light reflected from the magnetic layer is rotated at an angle called the Kerr rotation, with a typical value of 1° for the recorded area and an opposite rotation for the erased area. This difference is detected for the signal readout. Recording on an MO disk is called thermomagnetic recording because the magnetization is reversed at an area heated by laser irradiation where the coercivity at the elevated temperature is decreased below the external magnetic field (see Fig. 9.36b). The recorded mark has a magnetization upward, opposite to the erased state. A typical amorphous $Tb_{20}Fe_{74}Co_6$ recording layer (see Fig. 9.36a) has a high perpendicular anisotropy constant K_U of several 10^6erg/cm^3, which originates from the large magnetostriction coefficient and the large single-ion anisotropy of Tb, and a Tb spin directed opposite to the spins of the transition metals Fe and Co, giving rise to a ferrimagnetic behavior (Fig. 9.36a). Due to this behavior, the total magnetization approaches zero at the elevated temperature T_{comp} where it can be reversed by a moderate external field for recording (Fig. 9.36b). The recorded information is estimated to be stable for more than 100 years at ambient temperatures and a recording repeatability factor of more than 10^6 is achieved [9.103].

The storage capacity of MO disks has been favorably enhanced by the domain wall displacement detection (DWDD) technique. Here, the resolving power is not limited by the optical mark size but determined by the magnetic domain wall width which is estimated to 8 nm for Tb–Fe–Co (see Fig. 9.37a). DWDD technology has been used in high-density MiniDisks (HiMDs), which where commercialized in 2004 with storage capacities of 1 Gbyte per 64 mm diameter disk [9.103].

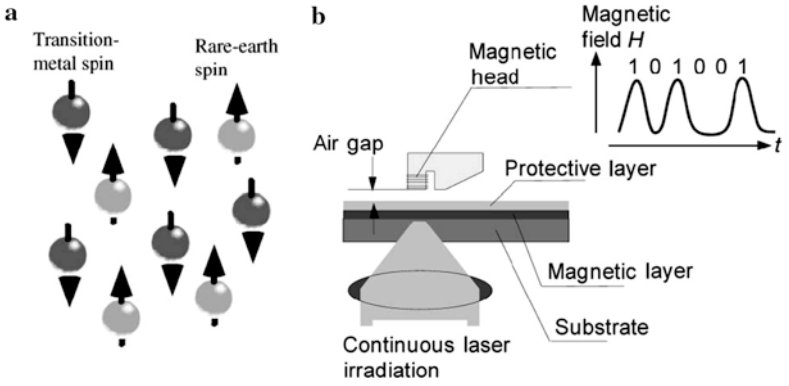

Fig. 9.36 (**a**) Antiparallel alignment of the magnetic moments of a ferrimagnetic rare-earth/transition-metal amorphous alloy. (**b**) Recording on a magneto-optical storage device by magnetic field modulation. H is the magnetic field and t is time. (Reprinted with permission from [9.103]. © 2006 Materials Research Society)

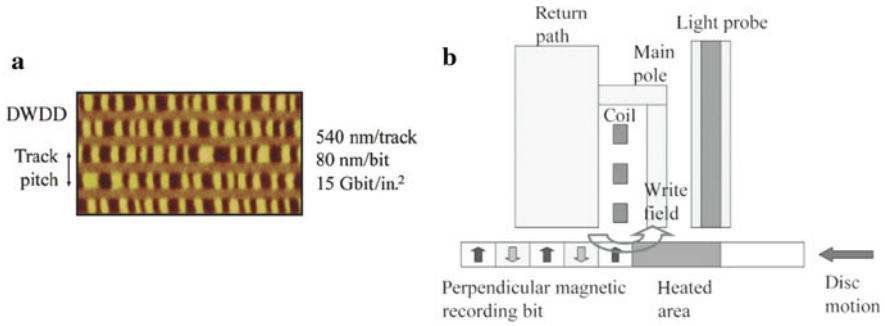

Fig. 9.37 (**a**) Magnetic force micrograph of recorded magnetic domains for domain wall displacement detection (DWDD) in magneto-optical data storage. Dark and light areas refer to two opposite magnetization directions. The track pitch for the DWDD media is 540 nm. (**b**) Schematic configuration for hybrid recording. (Reprinted with permission from [9.103]. © 2006 Materials Research Society)

Various MO technologies, including perpendicular recording media, are anticipated to achieve an areal density of 1 Tbit/in^2 [9.103]. For these high data storage densities, the coercivities H_C of the magnetic marks have to exceed 800 kA/m (10 kOe) in order to ensure the thermal stability at small sizes. In this case, heat-assisted recording, for reduction of H_C during recording (Fig. 9.37b) has been proposed, similar to the suggestion for high-density magnetic recording (see Sect. 9.5).

9.6.3 Multilayer Recording

The capacity of optical disks can be also increased by using multiple layers of bitwise data. Layers are spaced along the depth dimension of the disks (Fig. 9.38).

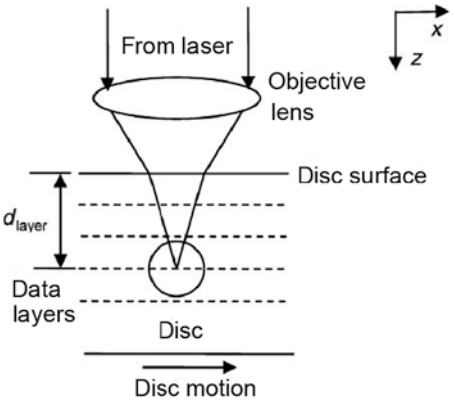

Fig. 9.38 Geometry of a bitwise volumetric optical data storage device. A data layer (*dashed lines*) is accessed by focusing a laser beam to different depths, d_{layer}. Readout is performed in reflection. (Reprinted with permission from [9.104]. © 2006 Materials Research Society)

Individual layers are recorded and information is retrieved in a manner that is very similar to conventional optical disk systems using a single layer. Bitwise volumetric multilayer recording is different from volumetric holographic recording (see below), in that holographic recording stores data as collections of gratings throughout the depth of the material.

In multilayer recording, two-photon (2P) absorption is used for the writing process (see [9.104]). The advantage of a 2P absorption process is its ability to selectively excite molecules inside the focus volume, e.g., of a short-pulse high-irradiance laser, without affecting molecules elsewhere in the storage material [9.104]. Data readout is often a simple one-photon process, because depth-discriminating techniques, such as scanning confocal microscopy, can be used.

For recording media, several categories of materials can be used including refraction near-field structure (super-RENS) materials, and thin-film refractive layers. To date, the most mature bitwise volumetric technology uses two-photon fluorescent media (see [9.104]).

9.6.4 Holographic Data Storage

Holographic storage is considered a promising successor to currently available storage technologies because of recent demonstration of significant gains in data transfer rates, densities and archival storage robustness, however, with challenges in the development of suitable recording materials [9.4].

Optical holography, on which holographic storage is based, can record the complete characteristics of a light wave. This recording of information is accomplished by overlapping two coherent light waves to produce an interference pattern (Fig. 9.39). The intensity profile of the pattern, determined by both the phases and the amplitudes of the interfering light waves, is imaged into a recording medium to produce a hologram. Either light wave can be regenerated by illuminating the hologram with the other light wave. Applying the reference beam to the recording medium (Fig. 9.39b) diffracts the light from the hologram to reconstruct the original 3d object [9.105]. The classic treatment of the behavior of light diffracted from volume holograms is known as coupled wave theory [9.106]. As shown in Fig. 9.39, laser light in a holographic storage system is split into the two arms, a reference path and a signal path, of the recording system. Digital data is recorded in a pagewise fashion – the bits of information are grouped into arrays and the arrays are encoded onto the pixels of a spatial light modulator. Light transversing the signal path is, therefore, patterned by the digital data array, or page. The light from the signal path overlaps with the light from the reference path within the recording medium to record an optical interference pattern that contains the information of the data page. Data is read out by diffracting light from the reference path off the optical interference pattern within the media to reproduce the recorded data array, which is imaged unto a detector to reconstruct the digital data (see [9.4]). Instead of recording and reading out data in a serial, bitwise manner, holographic storage

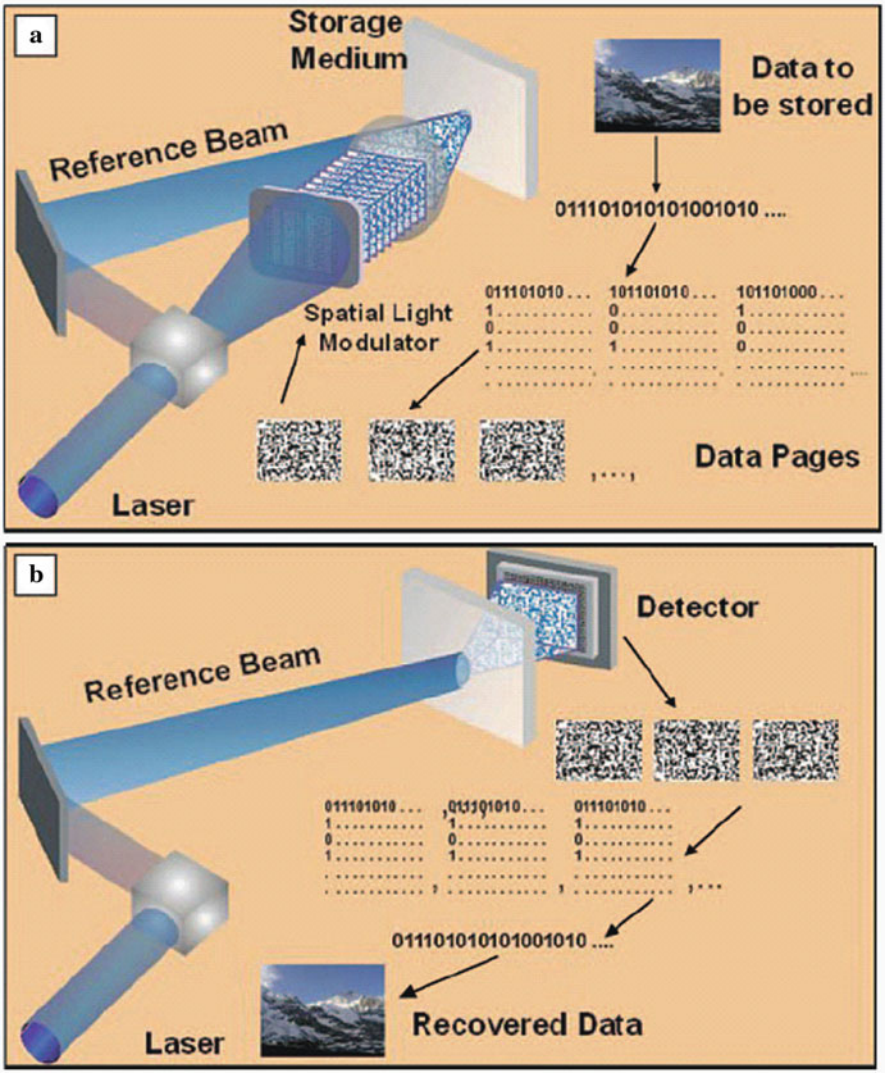

Fig. 9.39 Schematic illustrations of (**a**) the recording process in holographic storage and (**b**) the readout process in holographic storage. (Reprinted with permission from [9.4]. © 2006 Materials Research Society)

transfers data in a parallel, pagewise process, enabling significant improvements in recording and readout rates. In addition, holographic storage allows multiple pages of data to be recorded in the same volume of the recording media (multiplexing) enabling ultrahigh storage densities.

The requirements of the recording media are high optical quality, adequate dynamic range, high photosensitivity, long shelf and archival lives, and

manufacturability in a cost-effective manner [9.4]. Photopolymers with a two-chemistry approach can fulfill these requirements. These materials are, e.g., composed of two independently polymerizable systems – one system forms a 3D cross-linked polymer matrix, whereas the second photopolymerizable monomer is the imaging component, as it reacts during holographic recording. Using blue-wave length-sensitized, two-chemistry media with a 1.5 nm thick recording layer, 200 Gbits/in^2 was demonstrated [9.107]. From these materials, storage densities up to terabits/in^2 are expected [9.4].

9.7 High-*k* Dielectrics for Replacing SiO_2 Insulation in Memory and Logic Devices

In silicon-based information electronics, an important materials feature of silicon is, that it can be reacted with oxygen or nitrogen in a controlled manner to form superb insulators with excellent mechanical, electrical, and dielectric properties. These dielectrics are used as core components in two important device types in silicon semiconductor industry: as the capacitor dielectrics used for information storage in dynamic random access memories (DRAMs) and as the transistor gate dielectric in complementary metal oxide semiconductor (CMOS) field-effect transistor (FET) logic devices. In both cases, the thickness of the SiO_2 or Si–O–N dielectric is – with decreasing device size – becoming sufficiently thin (Table 9.4, Fig. 9.40a) that leakage currents arising from quantum mechanical electron tunneling through the dielectrics are posing a problem and are viewed as a major technical barrier [9.108–9.110]. When the thickness of the SiO_2 dielectric decreases below 1 nm, currents of a density of 1,000 A/cm^2 tunnel through the dielectric and increase by an order of magnitude when the dielectric thickness is reduced by a further 0.1 nm [9.110]. This gives rise to unacceptable energy consumption, cooling problems, and deleterious coupling between source-drain channel and gate. Continued device shrinkage will therefore require the replacement of the insulator with high-dielectric constant (high k) oxides [9.111], to increase its thickness, thus preventing tunneling currents while retaining the electronic properties of an ultrathin SiO_2 film ($k = 3.9$). Ultimately such insulators will require an atomically defined interface with silicon without an interfacial SiO_2 layer for optimal performance [9.109]. For application

Table 9.4 Roadmap predictions for dielectric gate oxide thickness (equivalent thickness of a SiO_2 dielectric) as a function of time (see [9.108])

Year	2005	2008	2011	2014
Technology node (nm)	100	70	50	35
Gate length (nm)	65	45	32	22
Equivalent oxide thickness (nm)	1.0–1.5	0.8–1.2	0.6–0.8	0.3–0.6

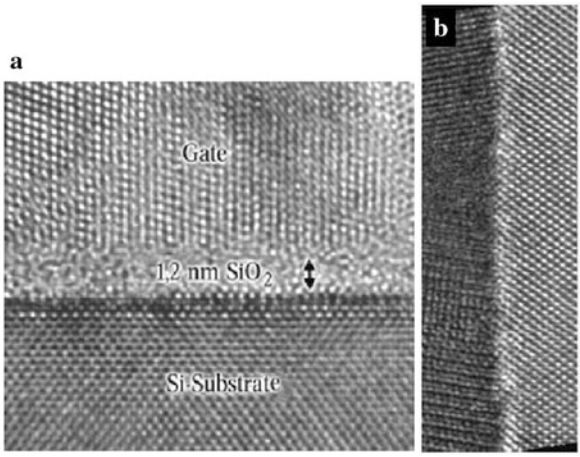

Fig. 9.40 (**a**) Transmission electron micrograph (TEM) of a cross section of a CMOS transistor in a Pentium-4 Processor (Intel Corp., see [9.110]). (**b**) High-resolution transmission electron micrograph (HRTEM) of the interface between a Si substrate (*right*) and a HfO_2 film (*left*), prepared at a deposition temperature of 350°C [9.116]. (Reprinted with permission from Refs. [9.110] (**a**) and [9.116] (**b**). © 2005 Wiley-VCH (**a**) and © 2009 Chinese Society of Metal (**b**))

as high-*k* insulators, amorphous Hf–Si–O–N compounds ($k \approx 11$–22) [9.112] and the application of oxides such as $LaAlO_3$ ($k \approx 25$) [9.113], Gd_2O_3 [9.114] or $LaLuO_3$ (see [9.111]) may enable industry companies to keep pace with Moore's law. High-quality oxide layers (see Fig. 9.40b) can be prepared by laser ablation techniques for highly precise compositional control and together with reflection high-energy electron diffraction (RHEED) techniques for structural control (see [9.110]). Processes for the preparation of ultrathin layers of high-*k* dielectrics have been reported [9.115].

High-*k* dielectric materials are used by Intel for transistors at the 45 nm technology node and by IBM for its 32 nm node CMOS technology [9.111].

9.8 Low-*k* Materials as Interlayer Dielectrics (ILD)

Modern ultralarge-scale integration (ULSI) electronic circuits contain 10^9 transistors in an area smaller than 1 cm^2. These basic elements must be interconnected and an advanced ULSI device may consist of 10 levels of metal lines. For this reason, the effective speed of the device is becoming ever more dominated by the signal propagation velocity through the interconnects of the components. The increase of the resistance (R) and the capacitance (C) of the interconnect materials give rise to a rapid increase in the delay time

$$RC = 2\rho k\varepsilon_0(4L^2/P^2 + L^2/T^2),$$

where ρ is the metal resistivity, ε_0 the vacuum permittivity, k is the relative dielectric constant of the interlayer dielectric (ILD), P is the metal line pitch (sum of line width and line spacing), T is the metal thickness, and L is the metal line length. Therefore, the device speed, increased through smaller feature sizes, will become overshadowed by this interconnect delay [9.117, 9.118]. The International Technology Roadmap for semiconductors (ITRS) predicts the necessary (maximum) k value of the ILD, and the estimated RC delay, for the various line width (DRAM half-pitch) "technology nodes", according to the expected year of production (see Fig. 9.41).

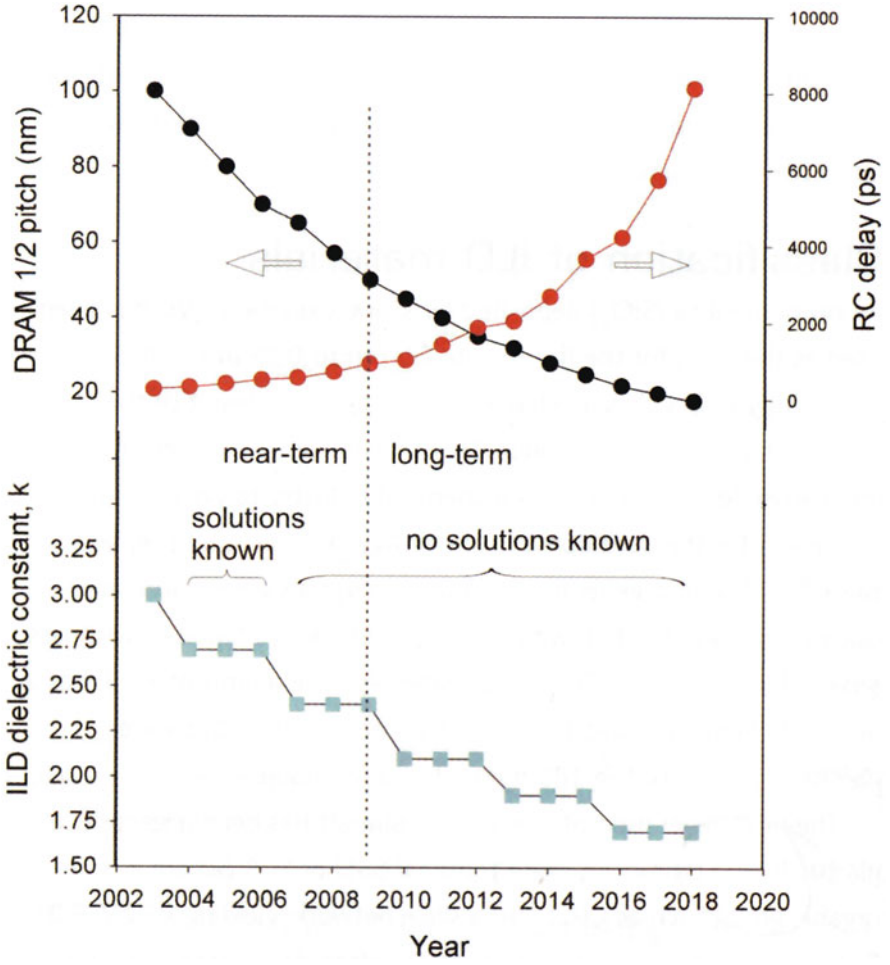

Fig. 9.41 The ITRS (2004 Update) industrial roadmap for the semiconductor industry, showing the planned decrease in device spacing (DRAM half-pitch), the expected increase in the RC delay, and the required k values of the interlayer dielectric (ILD), indicating the extent to which manufacturable solutions are known. (Reprinted with permission from [9.118]. © 2006 Elsevier)

Future low-*k* materials for ILDs [9.119] are porous materials such as periodic mesoporous organosilicas (PMOs; see [9.118, 9.120]) which are produced by template-based synthesis making use of bridged-organic silsesquioxane (SSQ) precursors to incorporate organic groups directly into the pore or channel walls (Fig. 9.42a). These PMOs have, however, polar silanol groups with OH bonds on the channel walls to be hydrophilic. The ingress of water with its high dielectric constant ($k \sim 80$) must be suppressed because this would cause the effective k to increase dramatically. This can be induced by thermal "hydrophobization" (Fig. 9.42b), where a proton from the hydrophilic hydroxyl group of a silanol (Si–OH) is transferred to a bridging group to break one Si–CH_2–Si bridge, thus creating a hydrophobic surface with terminal organic groups. This treatment causes k to decrease below 2.0 for the methenesilica, ethenesilica, and three-ring PMOs (see [9.118]). The film porosity – and thereby k – can be controlled by the template (surfactant)/precursor ratio R (see Fig. 9.42c) achieving values of $k \sim 1.75$ as required for ultralow-k ILDs. The mechanical properties of low-k dielectric materials are of importance for circuit reliability.

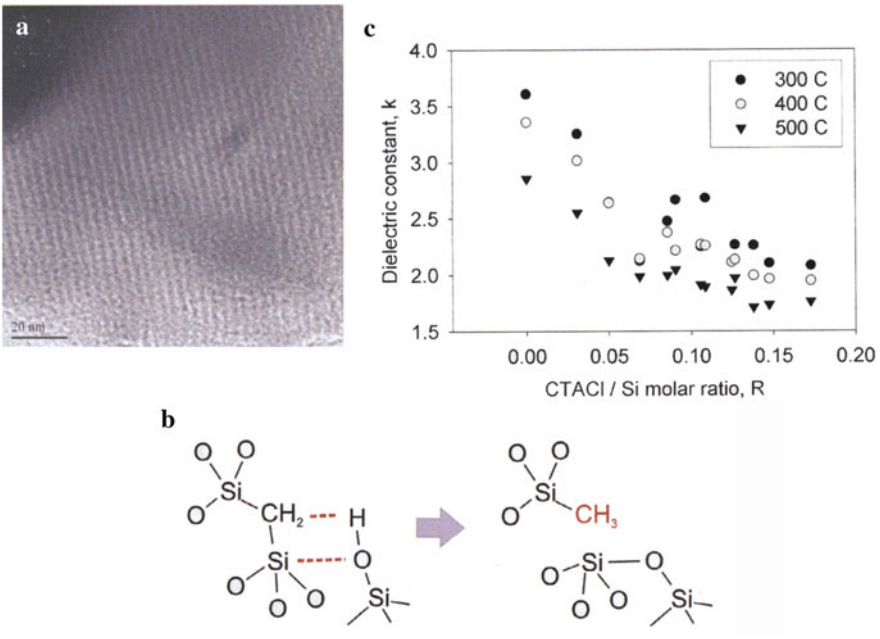

Fig. 9.42 (**a**) Transmission electron micrograph of periodic mesoporous organosilica (PMO) showing a 2D hexagonal structure of a ~ 4 nm channel spacing. (**b**) Illustration of the thermally activated chemical reaction that transforms an initial bridging organic group (*left*) to a terminal organic group (right), as a result of proton transfer from a silanol group in close proximity. (**c**) Decrease of the dielectric constant k for three-ring PMO films of increasing porosity as determined by the surfactant (CTACl)/precursor (Si-organo-of-silica) molar ratio R. The temperatures of the thermal treatments are given in centigrades. (Reprinted with permission from [9.118]. © 2008 American Institute of Physics)

9.9 Summary

The field of computer and data storage development with the fabrication of transistors or of data bits in storage media, respectively, is of particular importance for the application of nanoscience in computer industry with current revenues of US$ $\sim$ 200 billion annually. According to Moore's law the computing power – and in a similar fashion the data storage density – doubles about every 18 months due to a shrinkage of transistor sizes on an integrated circuit or of data bits to the nanometer scale. Due to physical limitations in the downscaling of transistors and data bits, novel strategies for the fabrication of these components have to be developed. Carbon nanotubes and graphene nanoribbons may provide us with future transistor technologies. Flash memories and magnetoresistive memories exhibit considerable downscaling potentials. With the implementation of nanoscale magnetic domain wall racetrack memories, the possibility of simplifying computers is opened by reducing the number of memory storage technologies. The storage capacity of magnetic hard disks could be dramatically increased by the use of GMR and TMR read heads based on nanoscale multilayers. For ultrahigh-density integration of computer components the development of high-dielectric constant (high k) and low-dielectric constant (low k) materials is indispensable.

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